



# H61H2-M2

Rev : 1.0

ECS CONFIDENTIAL

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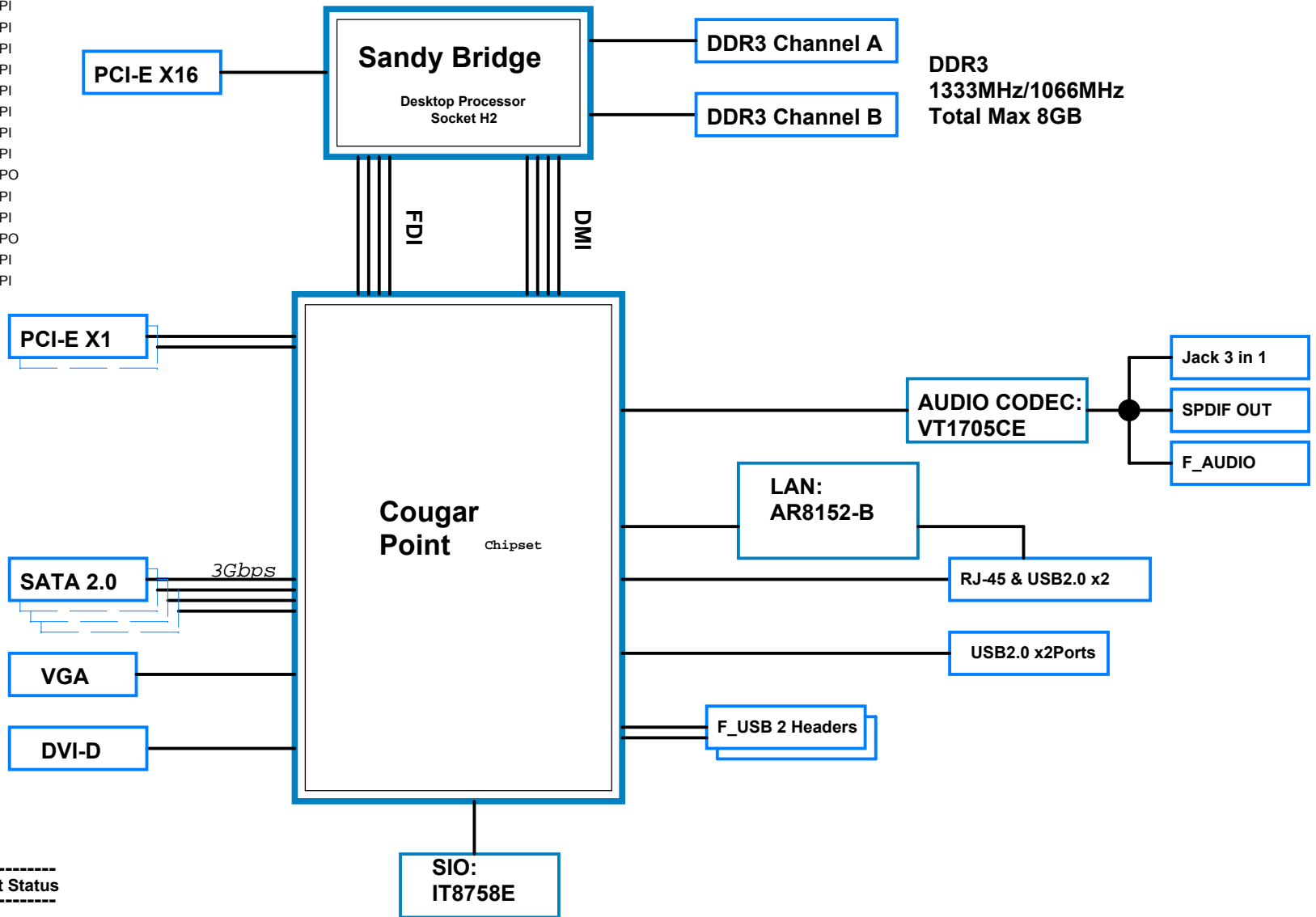
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Design by 428971\_428971\_Sugar\_Bay\_and\_BromolowWS\_PDG\_Rev\_0\_8.pdf,  
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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/09/23	Change from H67H2-M3 1. Audio change to vt1705 2. Super IO change to IT8758E 3. VCore PWM change to RT8859M 4. V_CPUVTT PWM change to RT8121 5. LAN change to AR8151-B & AR8152-B 6. Del PCI function 7. Del USB3.0 function 8. Del SATA 6G 9.Del Easy Charge Circuit of F_USB1
V.1.0	2010/12/03	1. PSON- Pull High 從5VSB改為3VSB_IO 2. Del EC33 1000U-6.3DL-O 3. Change EC35 from (1000U-6.3DL) to (820U-2.5D6-OS) 4. Del EC24 100U-16DE-O 5. 更改DDR3 SOCKET 顏色為兩根都灰色 6. 更改BATTERY SOCKET換成非架高料 7. 更改POWER CONN. 24pin 換成半透明STD料 8. 更改F_USB1改成和F_USB2為相同的顏色 9.VT1705更改為VT1705CE 10.SATA0GP、SATA1GP、SATA2GP、SATA3GP、SATA4GP、SATA5GP 增加Pull High & Low線路

## PCH-GPIO function

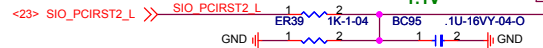
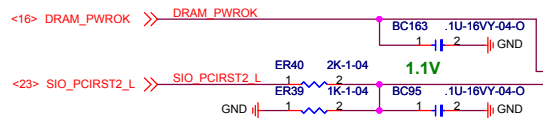
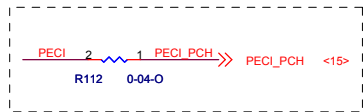
Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



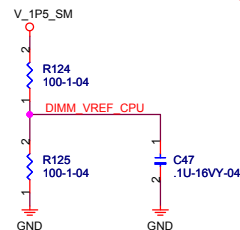


CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFSEL[0]
6	*	*	PEOFSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:  
 01=DEFAULT X16,  
 01=2X8,  
 10=RESERVED,  
 00=X8,X4,X4



change test point for internal PU Jack05/25

- STP1 ● 1 CFG 0 H36
- STP8 ● 1 CFG 1 J36
- STP16 ● 1 CFG 2 J37
- STP9 ● 1 CFG 3 K36
- STP20 ● 1 CFG 4 L36
- STP25 ● 1 CFG 5 N35
- STP19 ● 1 CFG 6 L37
- STP17 ● 1 CFG 7 M36
- STP21 ● 1 CFG 8 J38
- STP18 ● 1 CFG 9 L35
- STP28 ● 1 CFG 10 M38
- STP30 ● 1 CFG 11 N36
- STP33 ● 1 CFG 12 N38
- STP32 ● 1 CFG 13 N39
- STP34 ● 1 CFG 14 N37
- STP35 ● 1 CFG 15 N40
- STP7 ● 1 CFG 16 G37
- STP2 ● 1 CFG 17 G36

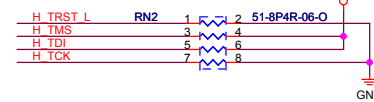
- AT14 RSVD\_016
- AY3 RSVD\_023
- H7 RSVD\_028
- H8 RSVD\_029

5 OF 10

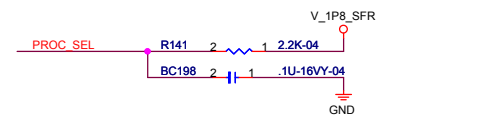
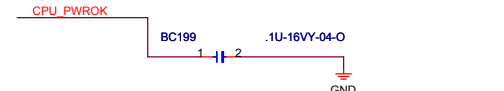
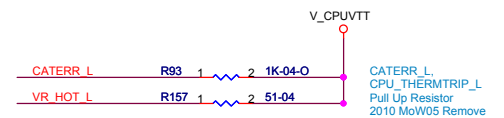
SKT\_H2\_CRB

CPUUE  
 BALLMAP\_REV=1.4

- VCCP\_SELECT P33 VTT\_SEL
- VCCSA\_VID P34 VCCSA\_VID <11>
- VCCSA\_SEN T2 VCCSA\_SEN <11>
- VCC\_SENSE A36 VCC\_SEN <9>
- VSS\_SENSE B36 VSS\_SEN <9>
- VCCIO\_SENSE AB4 VCCIO\_SEN <11>
- VSSIO\_SENSE AB3 VSSIO\_SEN <11>
- VCCAXG\_SENSE L32 VCCAXG\_SEN <9>
- VSSAXG\_SENSE M32 VSSAXG\_SEN <9>
- TDO L39 H TDO
- TDI L40 H TDI
- TCK M40 H TCK
- TMS L38 H TMS
- TRST# J39 H TRST\_L
- PRDY# K38 H PRDY\_L
- PREQ# K40 H PREO\_L
- DBR# E39 FP\_RST\_L
- RSVD\_001 C40 XDP H CLK DP
- RSVD\_002 D40 XDP H CLK DN
- BPM#\_0 H40
- BPM#\_1 H38
- BPM#\_2 G38
- BPM#\_3 G40
- BPM#\_4 G39
- BPM#\_5 E38
- BPM#\_6 E40
- BPM#\_7 E40
- RSVD\_024 B39
- RSVD\_030 J33
- RSVD\_037 L34
- RSVD\_036 L33
- RSVD\_033 K34
- RSVD\_040 N33
- RSVD\_039 M34
- RSVD\_018 AV1
- RSVD\_020 AW2
- RSVD\_038 L9
- RSVD\_032 J9
- RSVD\_034 K9
- RSVD\_035 L31
- RSVD\_050 J31
- RSVD\_053 K31
- RSVD\_051 AD34
- RSVD\_052 AD35

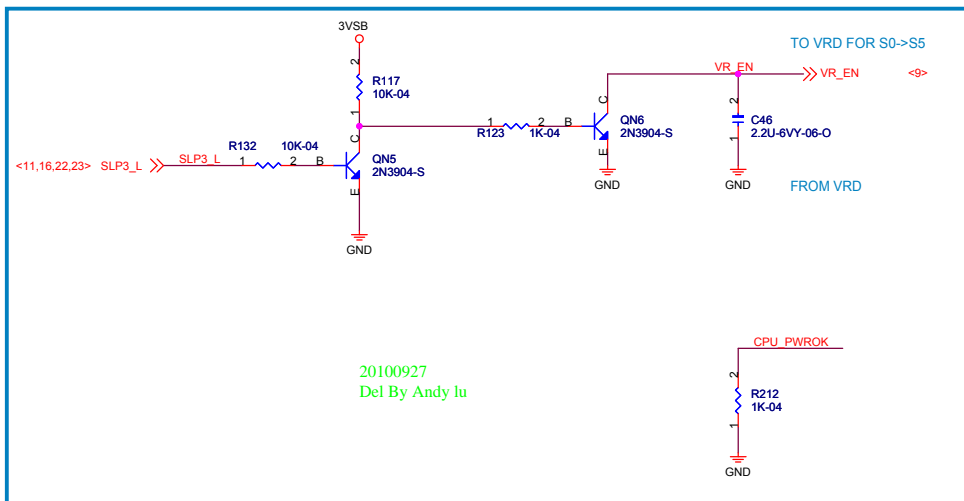


EDS P68/132 has internal PU Jack05/25

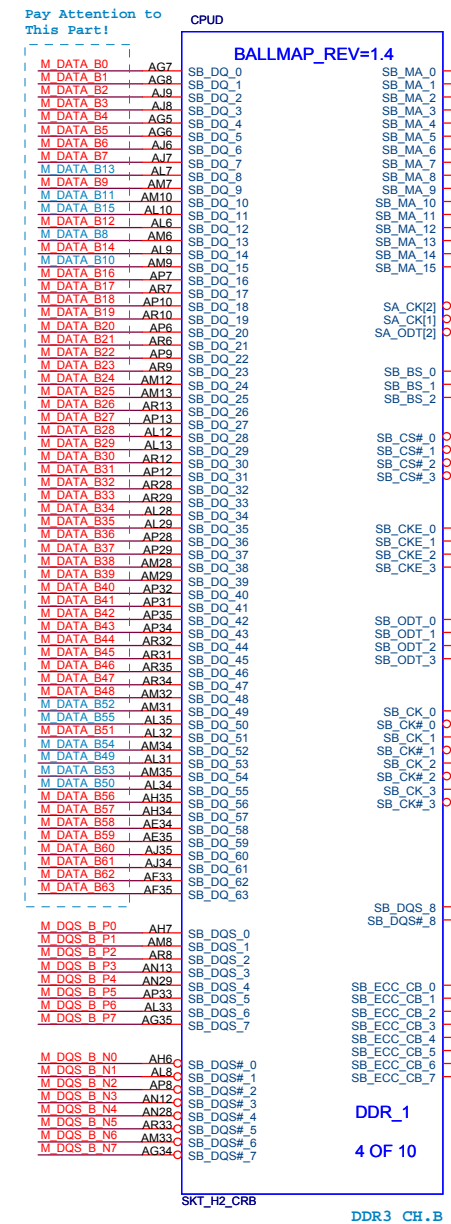
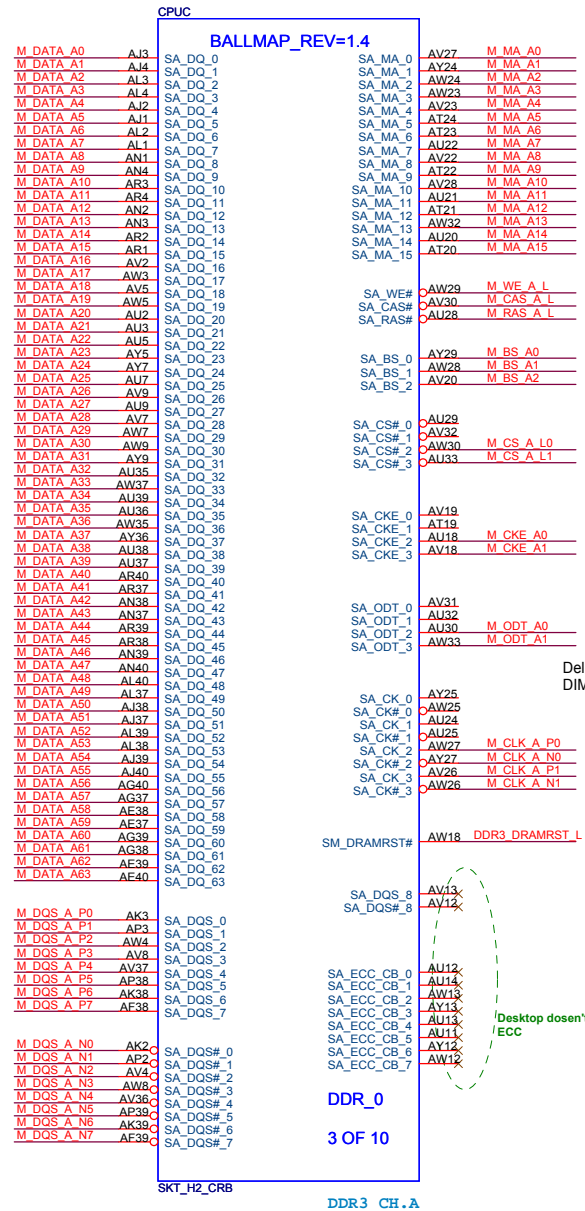
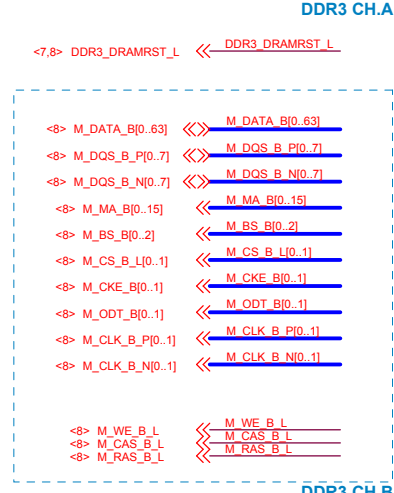
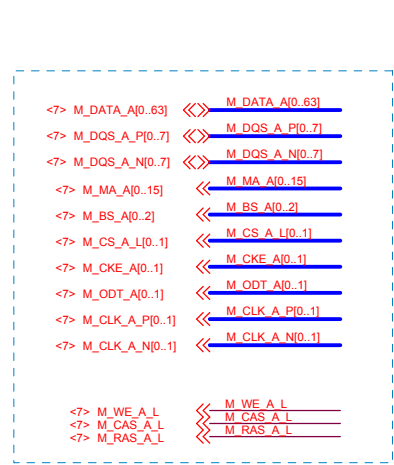


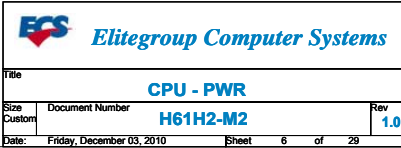
DMI/FDI termination voltage:  
 DC coupled: TX/RX to VCC ISF sampled high  
 DC coupled: TX/RX to VSS IF sampled low  
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

## Power Down Sequencing Circuit



20100927  
 Del By Andy lu

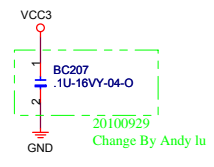
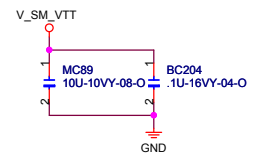
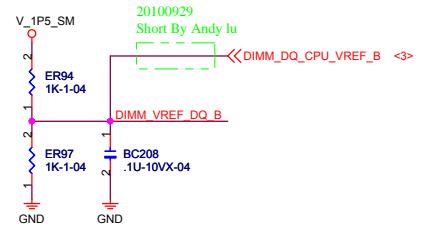
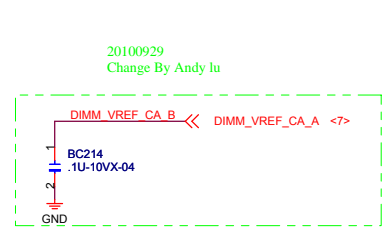
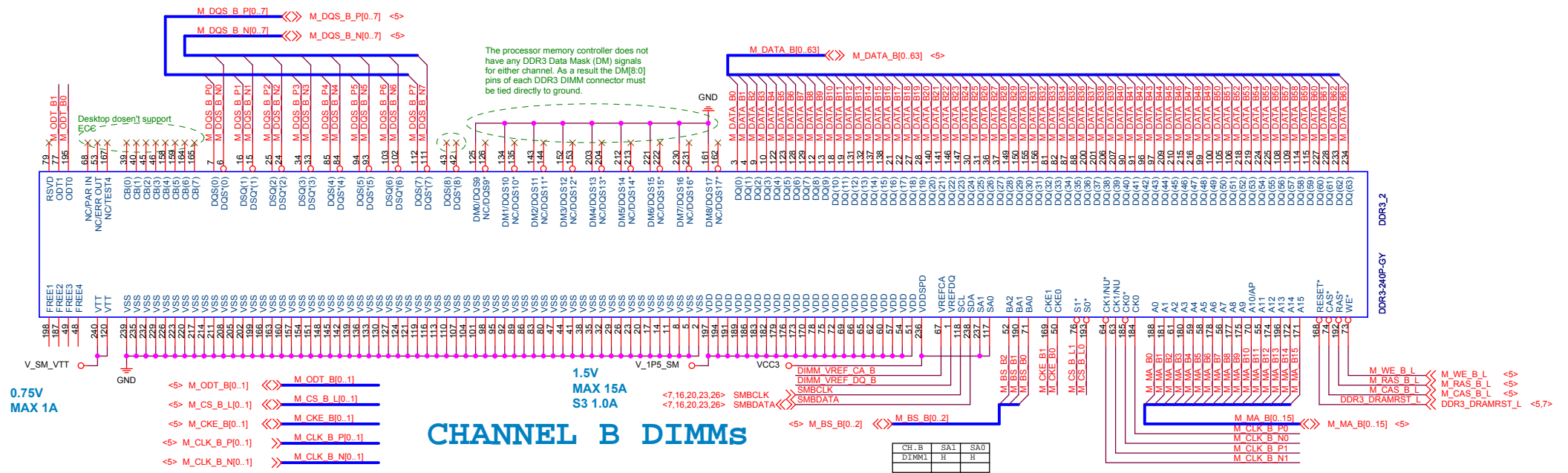








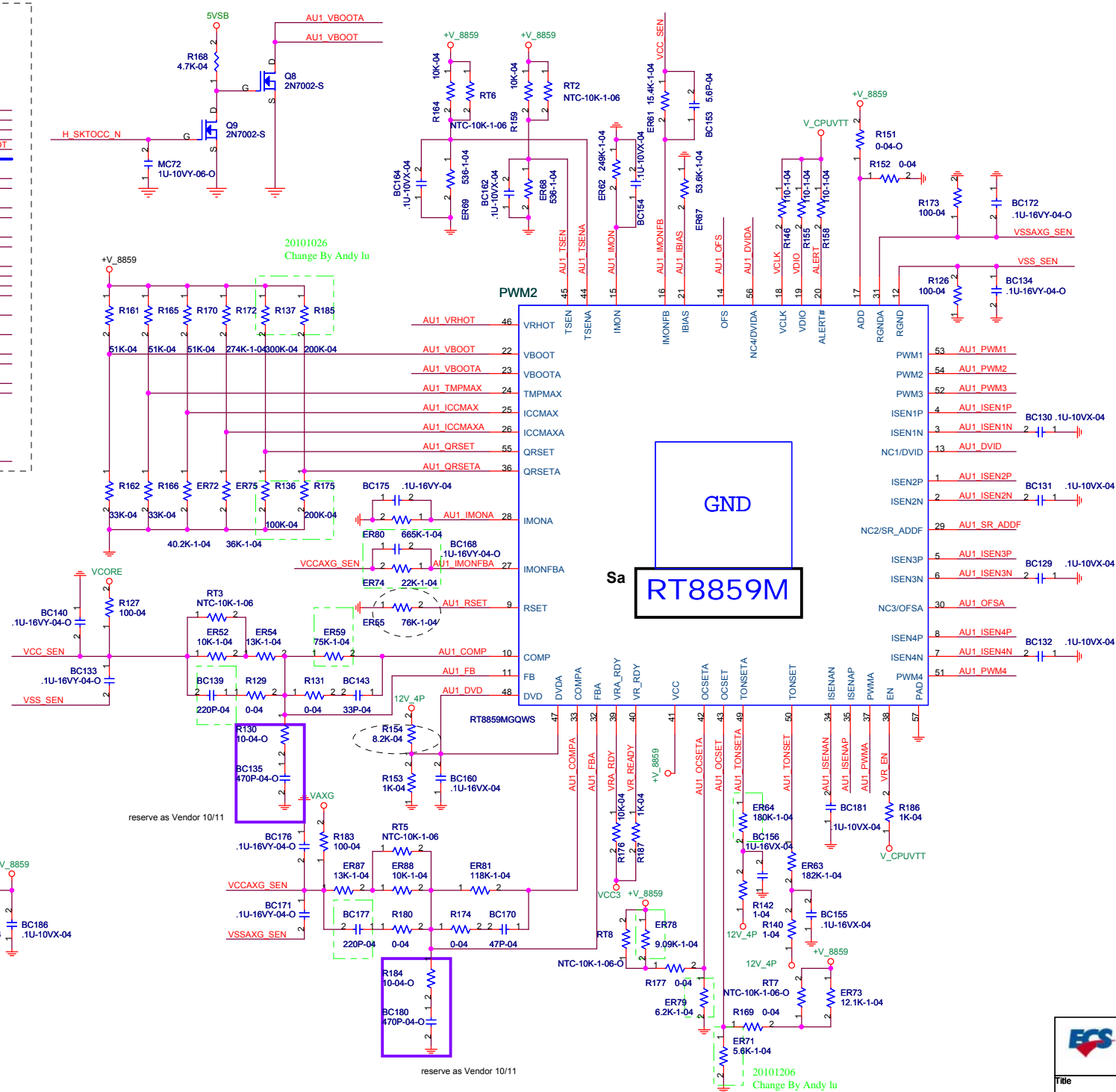
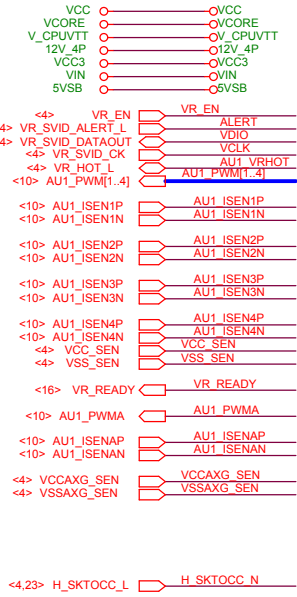
The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.



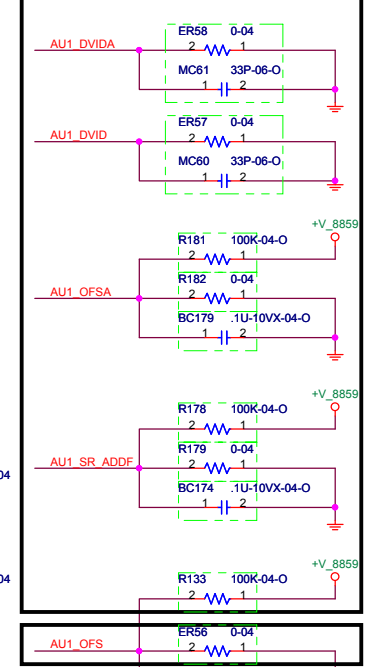
Del DIMM3 for always populate DIMM4 first Jack 05/13



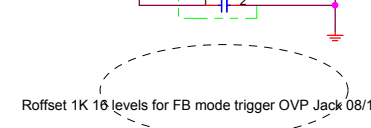
## External Connection



Sb



Sc



Rooffset 1K 16 levels for FB mode trigger OVP Jack 08/10

	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04	1K-1-04

change 1K for OVP

**Elitegroup Computer Systems**

Title: **DC/DC VCORE/VAXG RT8859M**

Size: Document Number **H61H2-M2** Rev **1.0**

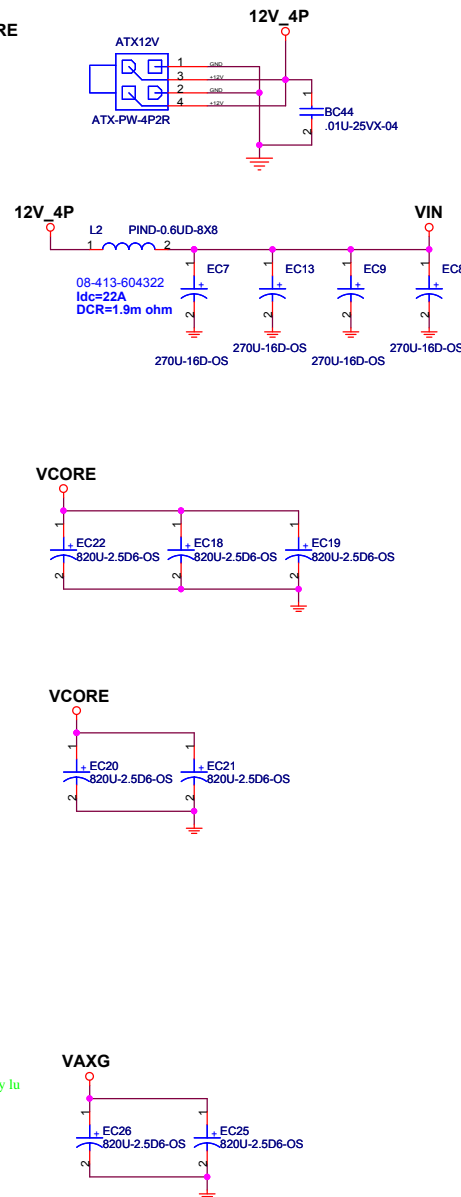
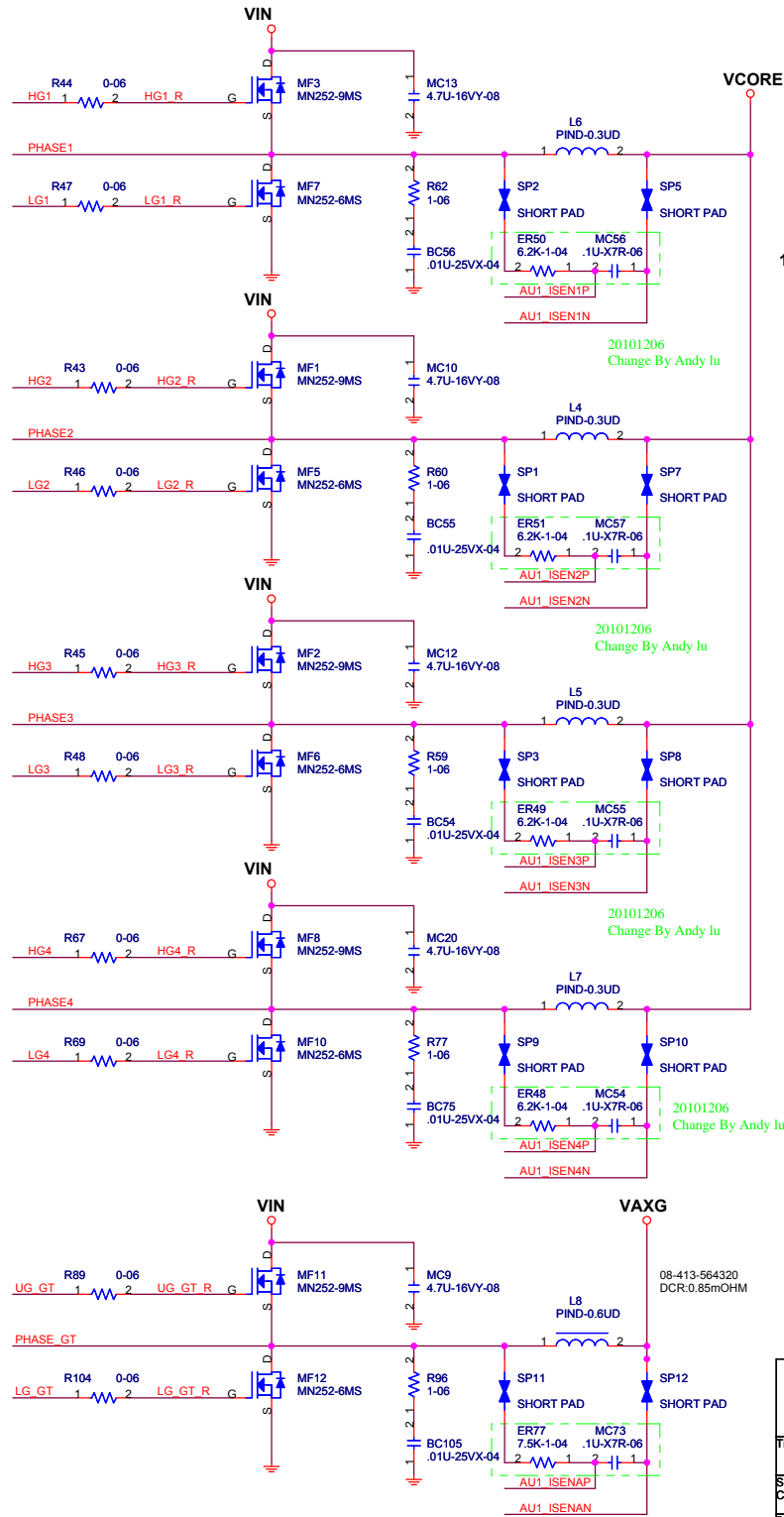
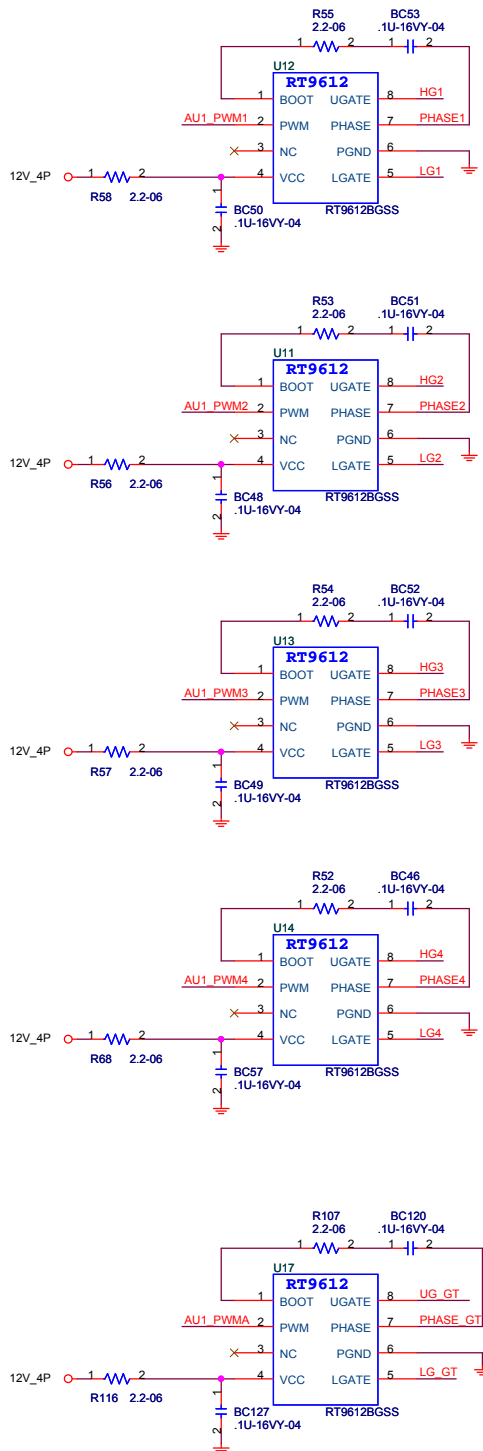
Date: Monday, December 06, 2010 Sheet 9 of 29

## External Connection

VCC ○ VCC  
VCORE ○ VCORE  
12V\_4P ○ 12V\_4P  
VCC3 ○ VCC3  
VIN ○ VIN  
VAXG ○ VAXG

<9> AU1\_PWM[1..4] ○ AU1\_PWM[1..4]  
<9> AU1\_ISEN1P ○ AU1\_ISEN1P  
<9> AU1\_ISEN1N ○ AU1\_ISEN1N  
<9> AU1\_ISEN2P ○ AU1\_ISEN2P  
<9> AU1\_ISEN2N ○ AU1\_ISEN2N  
<9> AU1\_ISEN3P ○ AU1\_ISEN3P  
<9> AU1\_ISEN3N ○ AU1\_ISEN3N  
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<9> AU1\_ISEN4N ○ AU1\_ISEN4N

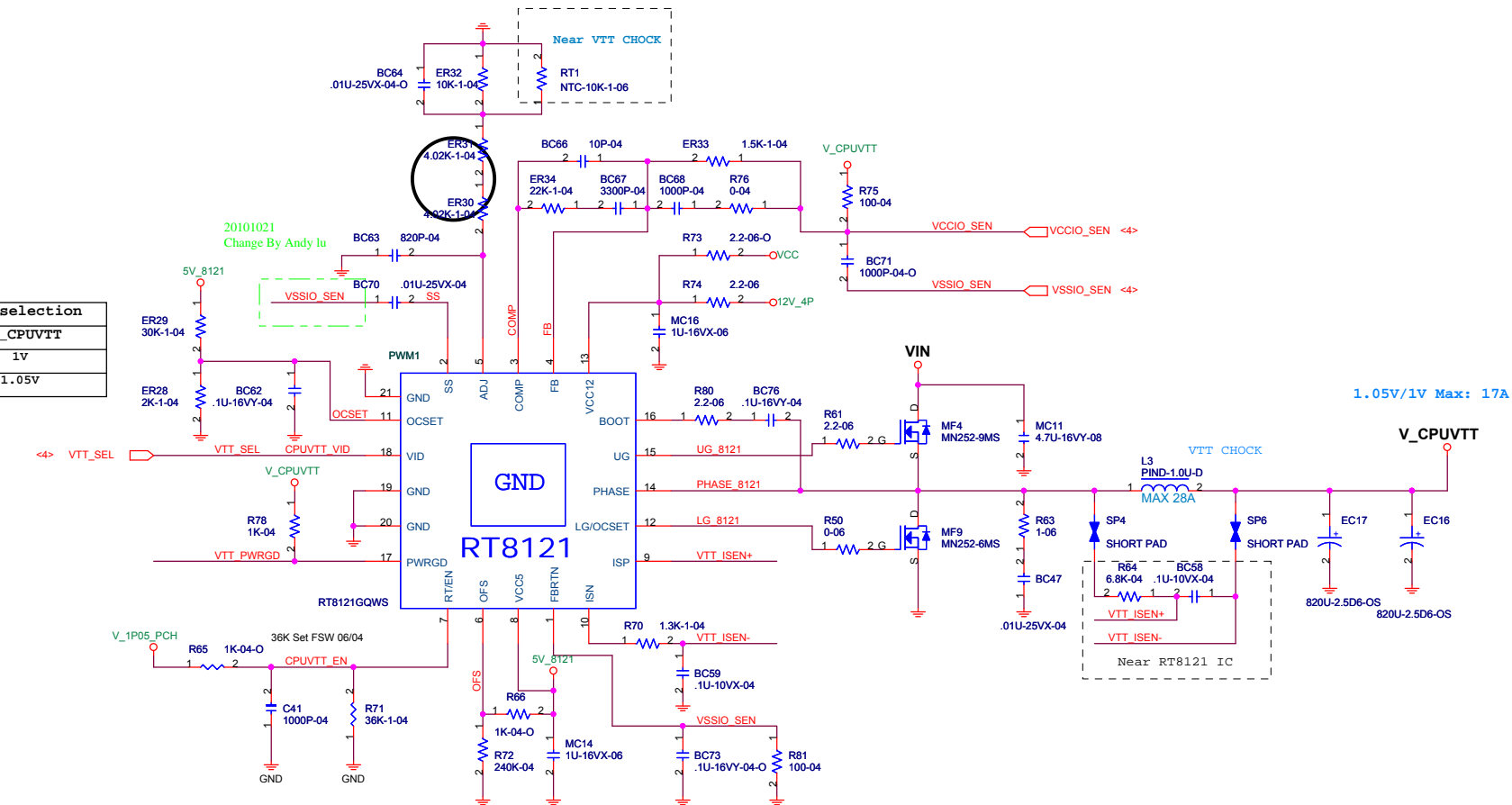
<9> AU1\_PWMA ○ AU1\_PWMA  
<9> AU1\_ISENAP ○ AU1\_ISENAP  
<9> AU1\_ISENAN ○ AU1\_ISENAN



## External Connection

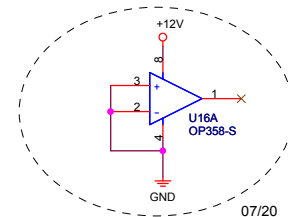
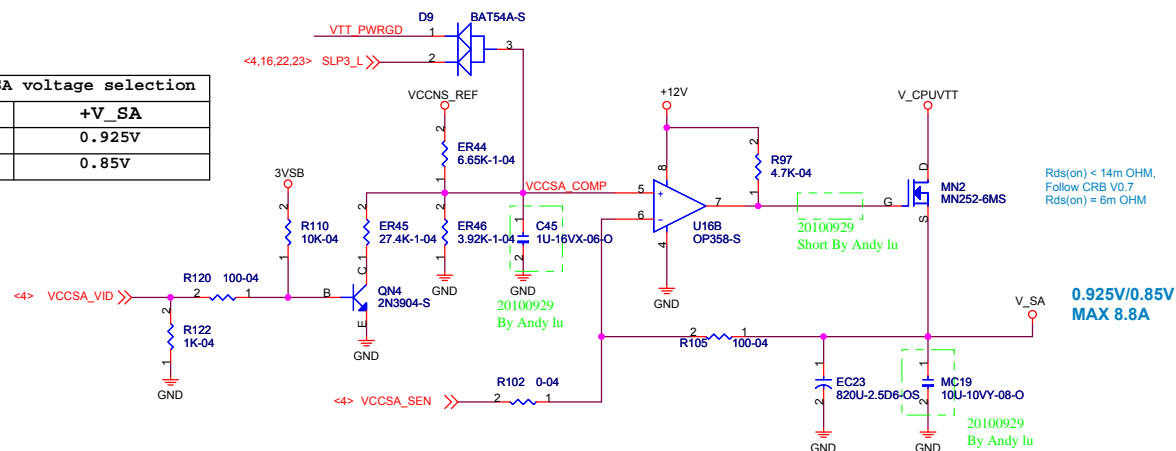
VCC ○ VCC  
 3VSB ○ 3VSB  
 5VSB ○ 5VSB  
 V\_1P05\_PCH ○ V\_1P05\_PCH  
 V\_CPUVTT ○ V\_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



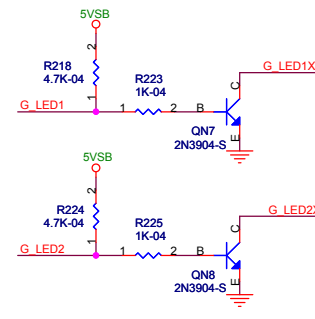
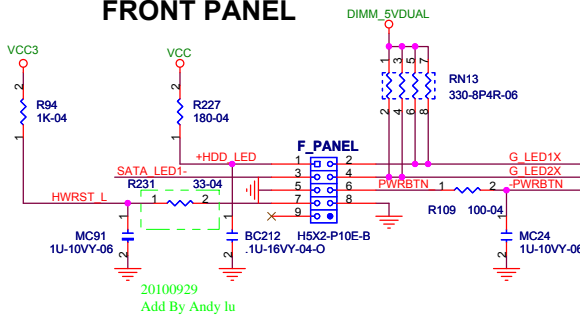
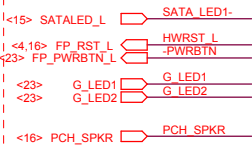
\* VCCSA voltage selection

VID	+V_SA
0	0.925V
1	0.85V



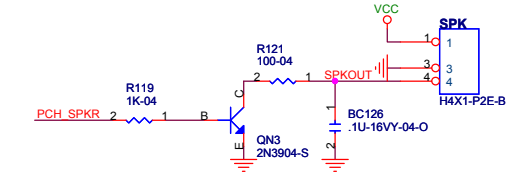


## External Connection



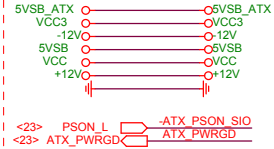
	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
G	GB	YB	OFF	OFF	OFF

B: Blinking



## POWER CONNECTOR

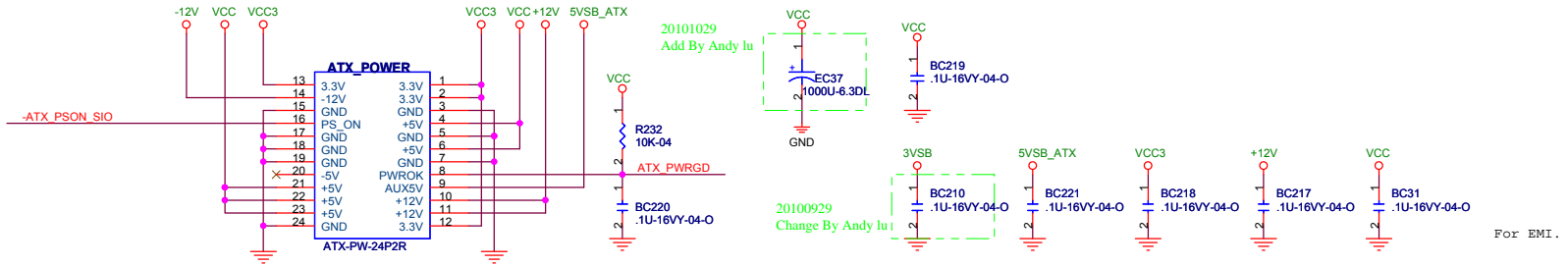
### External Connection



**F\_PANEL**

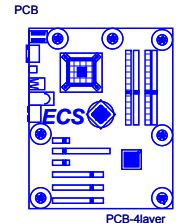
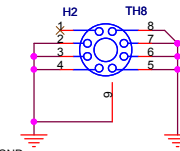
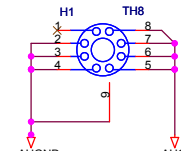
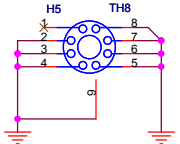
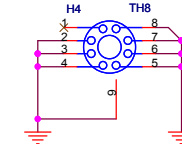
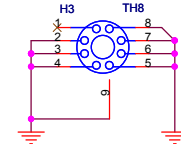
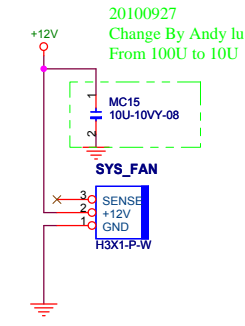
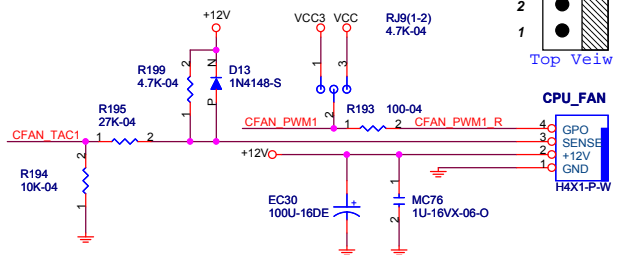
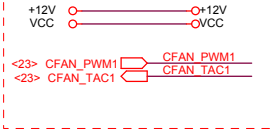
1	2	+ISOL
3	4	
5	6	PWR
7	8	
9	X	

REST



## FAN

### External Connection



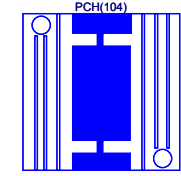
**PCB STACK:**

L1:TOP

L2:PWR

L3:GND

L4:BOTTOM



20-120-011476

5series PN:20-120-010851



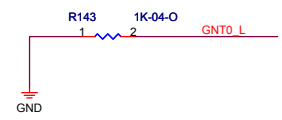
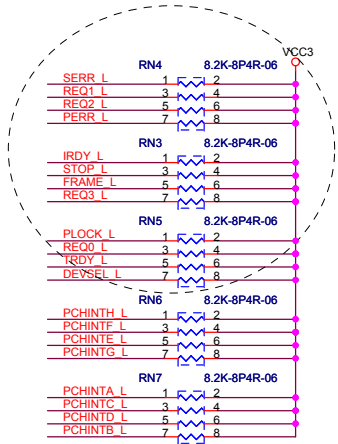
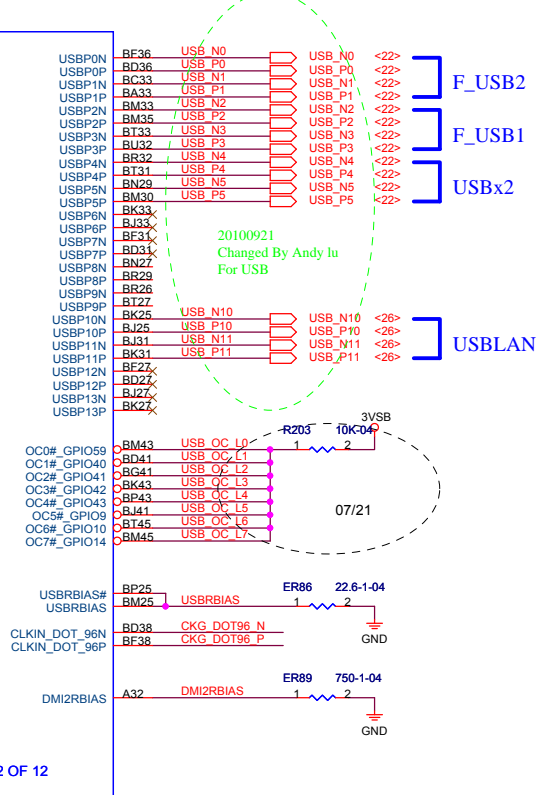
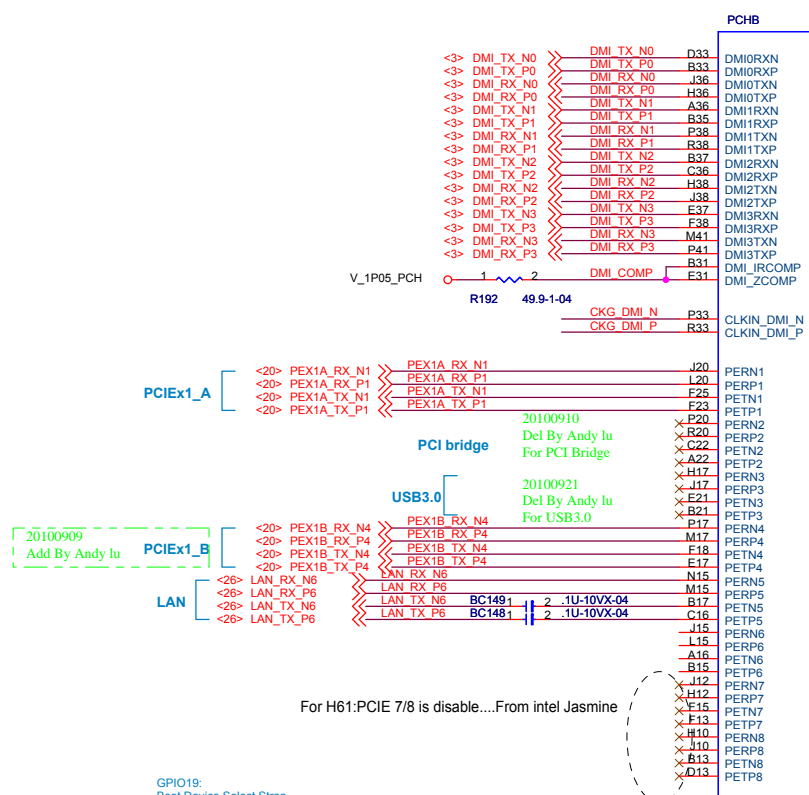
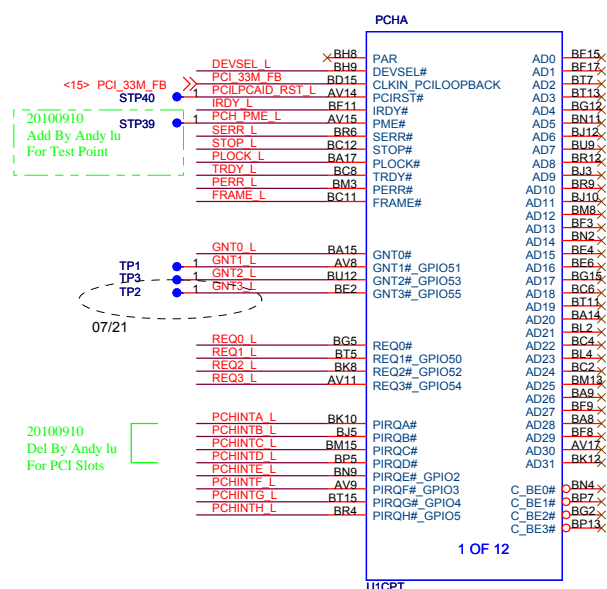
**Elitegroup Computer Systems**

Title: Front Panel,FAN,PowerConn,GND,104

Size: Document Number: H61H2-M2 Rev: 1.0

Date: Thursday, December 09, 2010 Sheet: 13 of 29

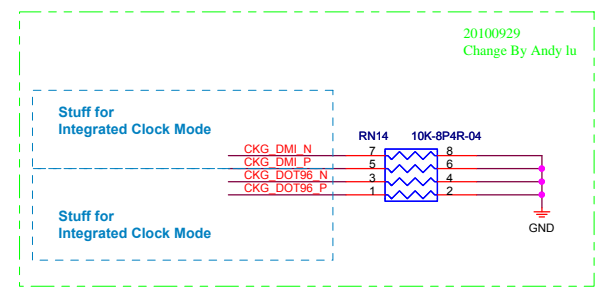
For H61:USB Port 6/7/12/13 is disabled....From 440377 file



GNT[0..3]#  
GPIO19  
have been internal pull high to +VCC3

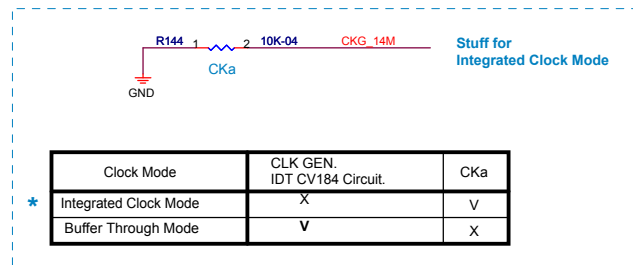
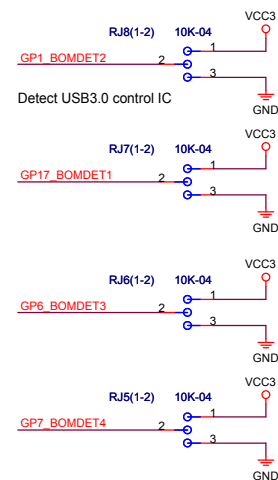
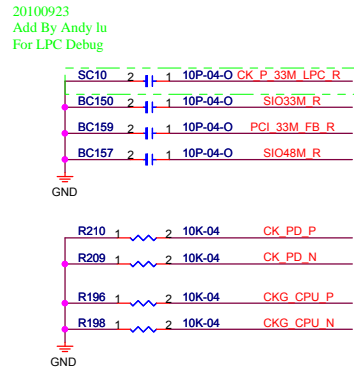
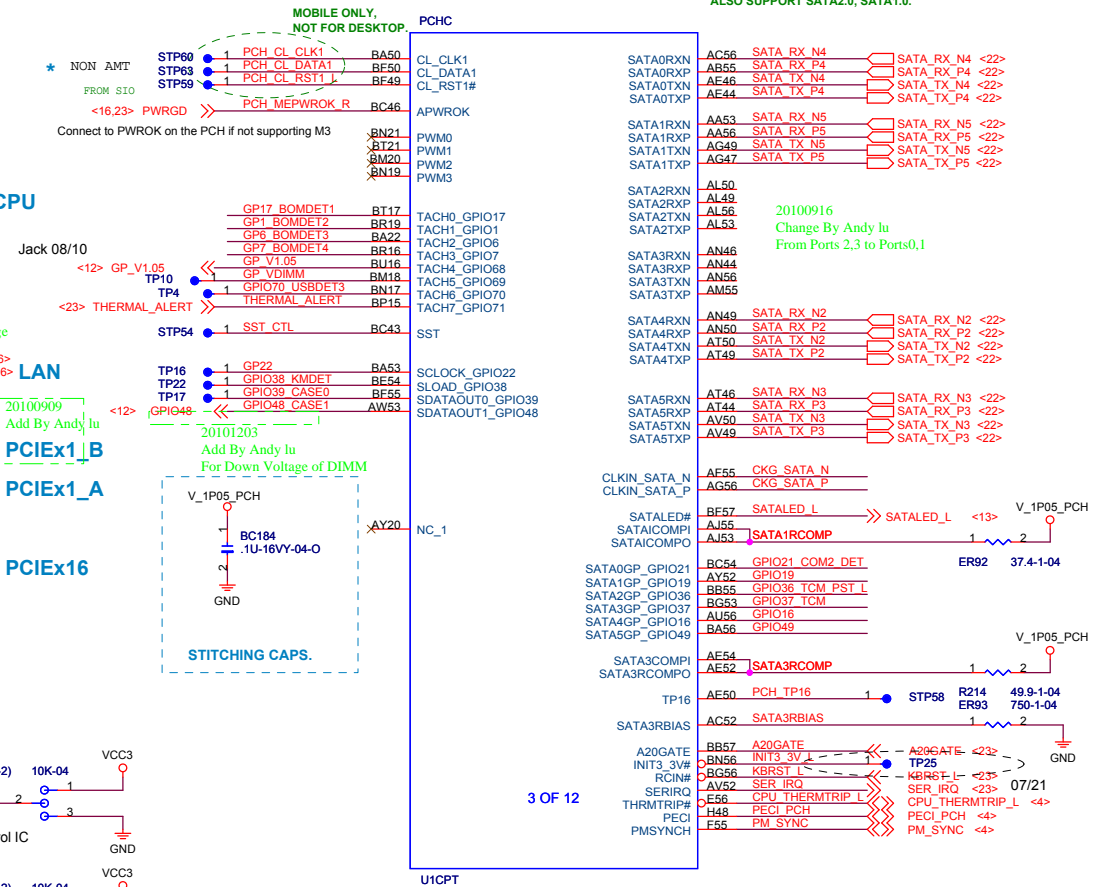
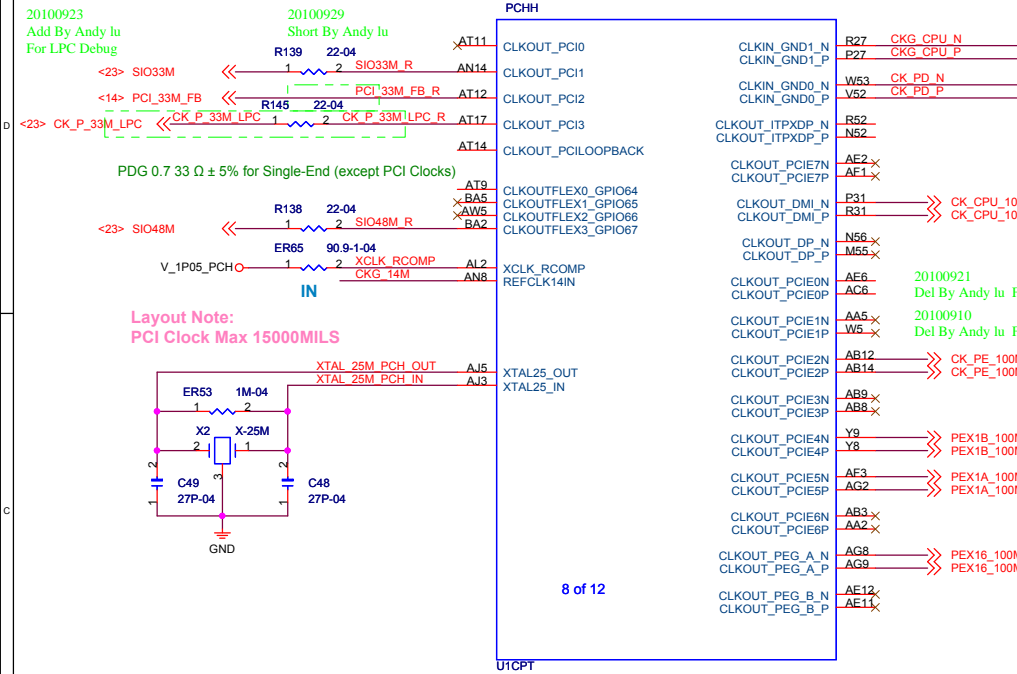
Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

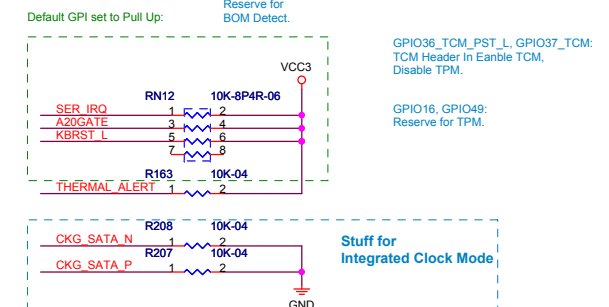
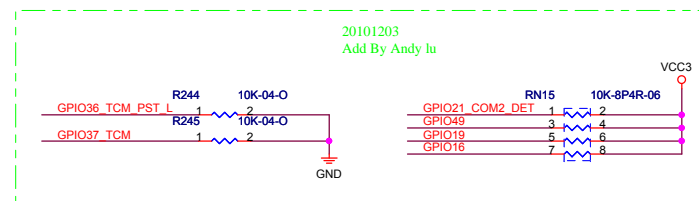


For H61:SATA port2/3 is disable....From 440377 file

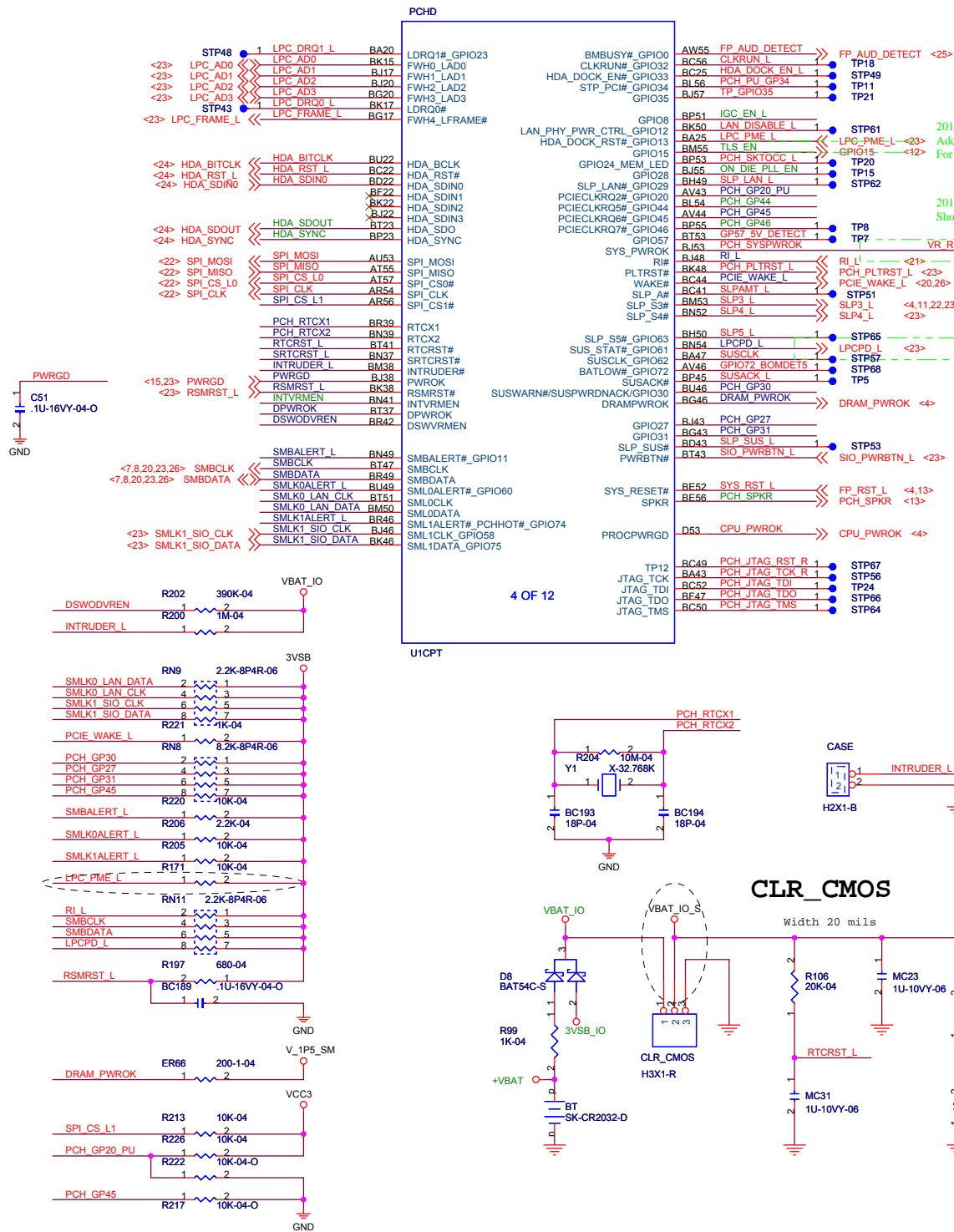
**ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,  
ALSO SUPPORT SATA2.0, SATA1.0.**



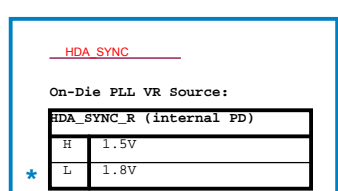
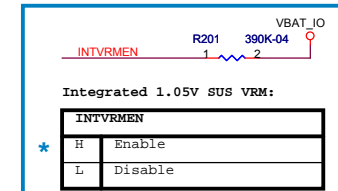
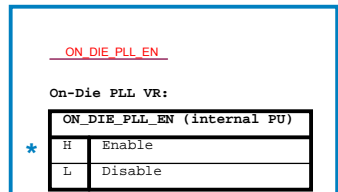
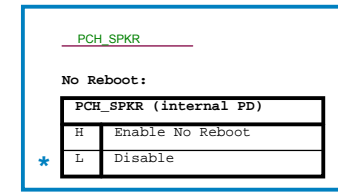
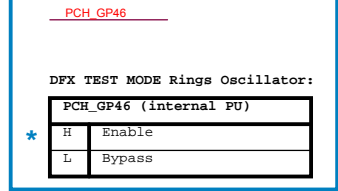
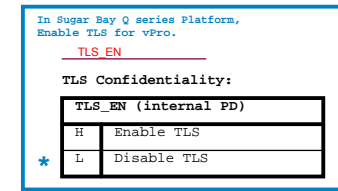
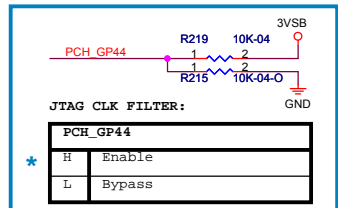
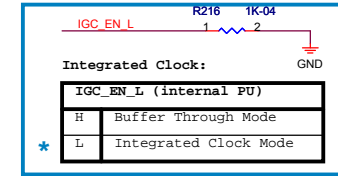
Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X



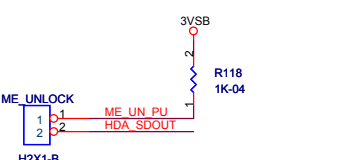
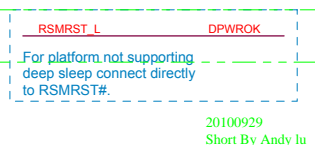




Buffer Through Mode / Integrated Clock Mode have been changed to F/W Strap. Default: Integrated Clock Mode. Doc. Cougar Point Platform Controller Hub (PCH) Family EDS Update V0.7.1

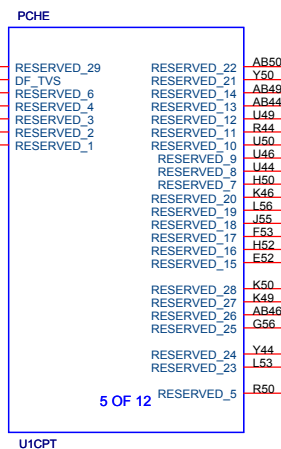


When Deep Sleep not implemented:  
1.PCH\_GP30, PCH\_GP27 need to be Pull Up.  
2.VCC0SDW3\_3 should to be connected to +3VSB.  
3.SLP\_SUS\_L, SUSACK\_L left unconnected.  
4.SUSWARN\_L may be used as GPIO30.(Reference to 1.)



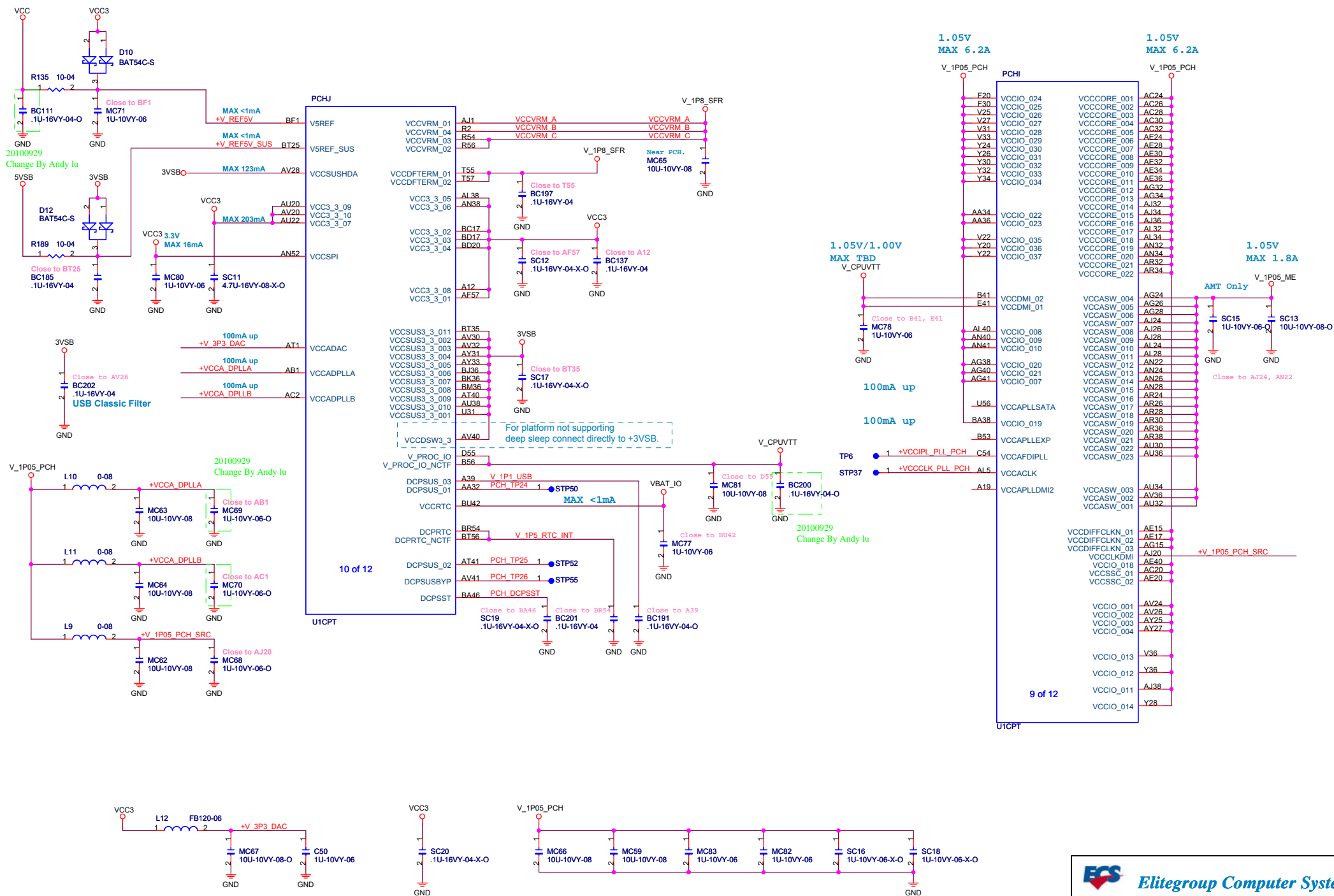
ME Enable/Disable

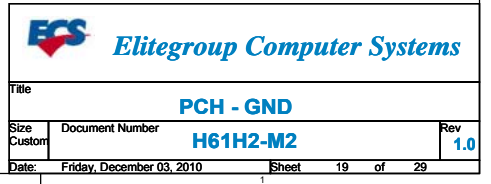
	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

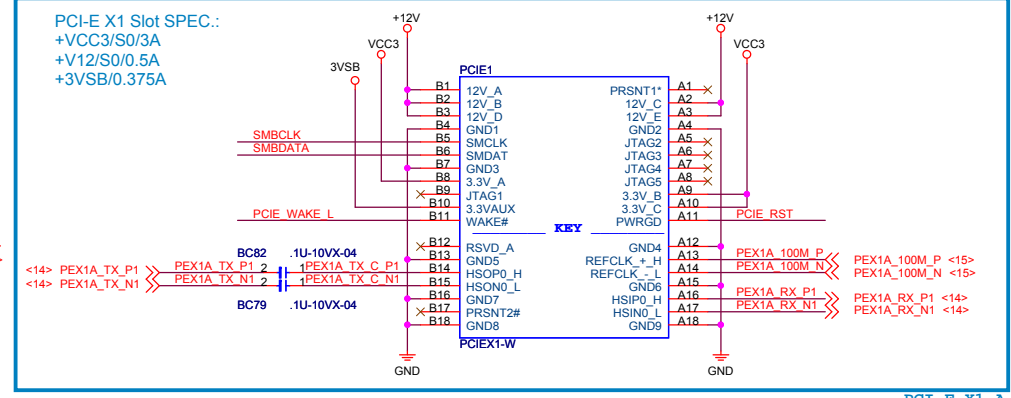
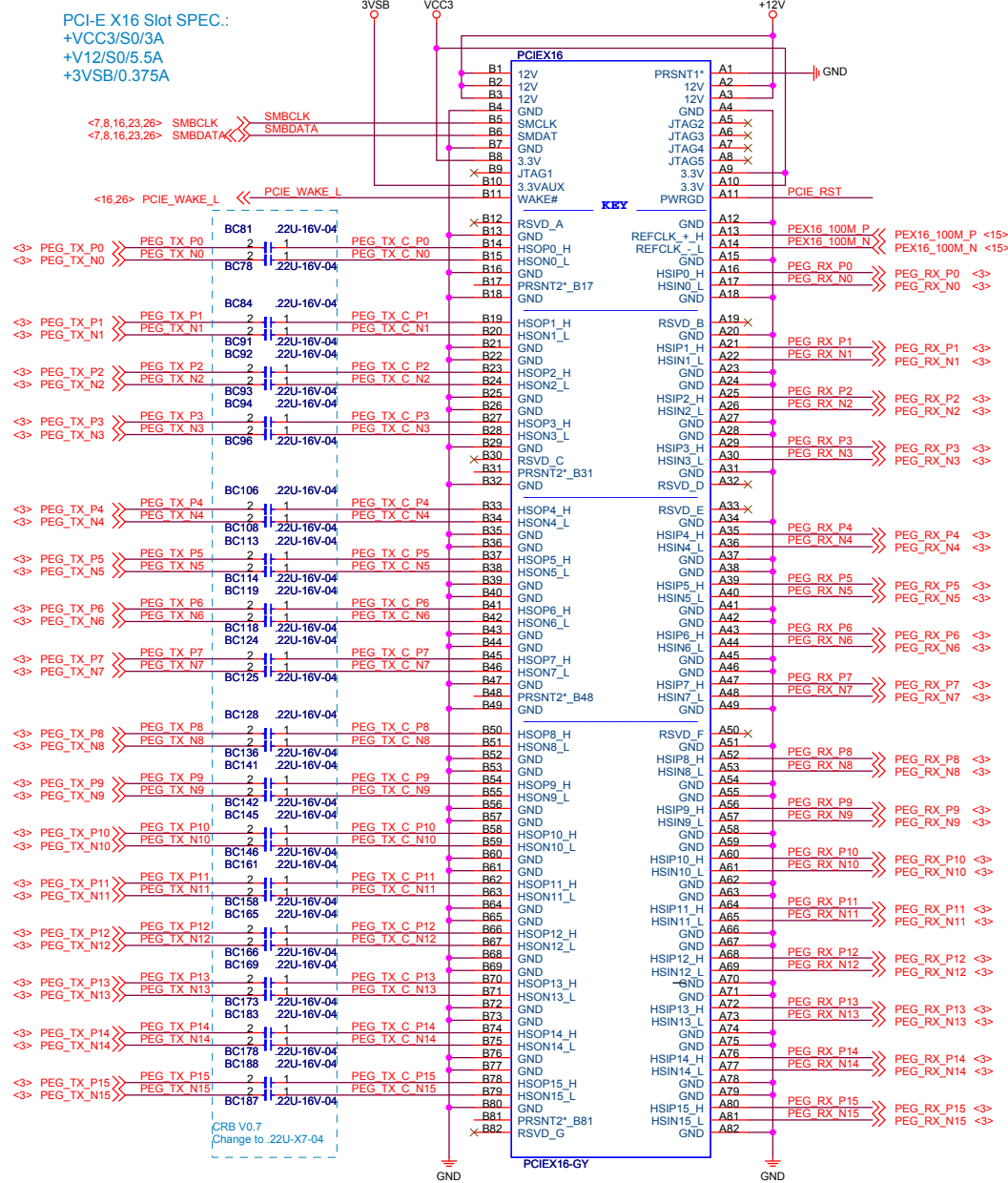


Renamed NV\_CLE to DF\_TVS.

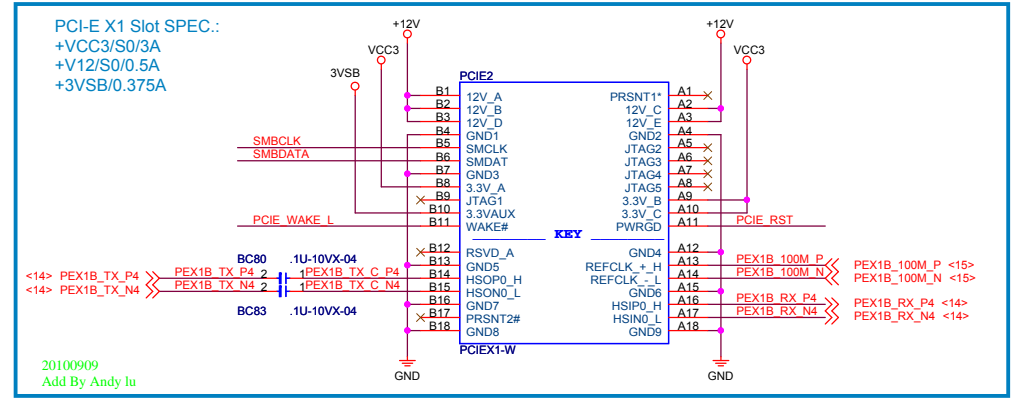




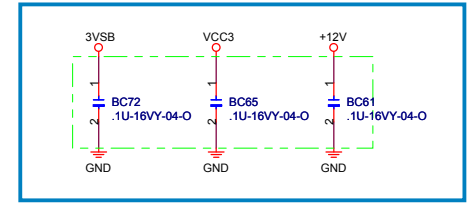




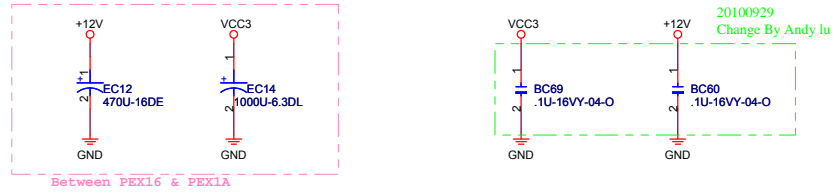
PCI-E X1 A



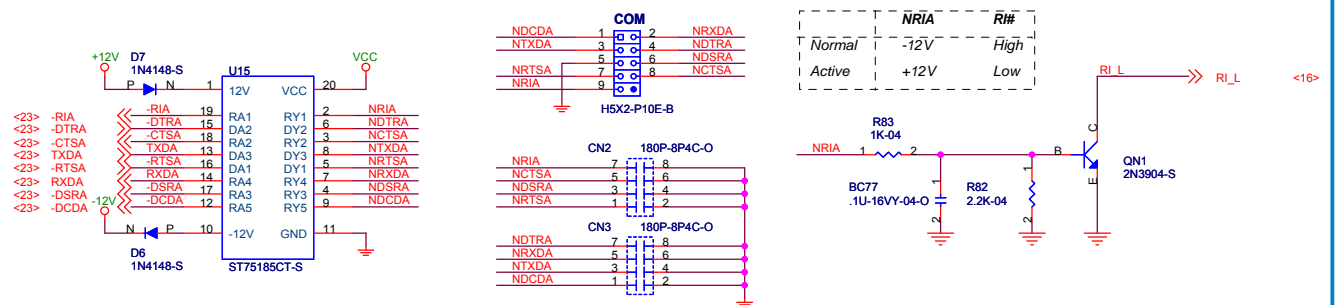
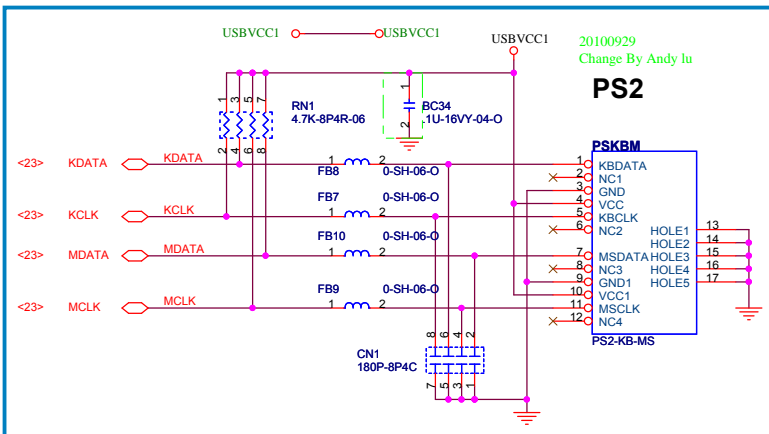
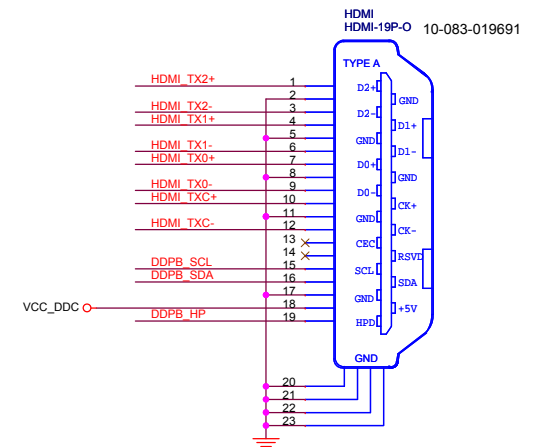
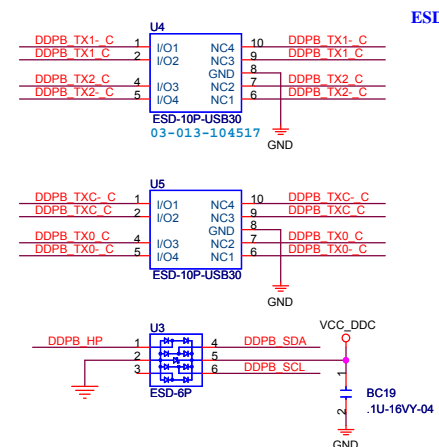
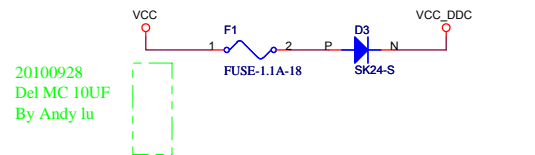
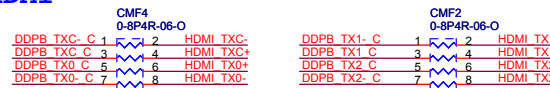
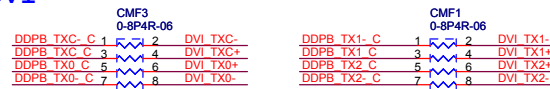
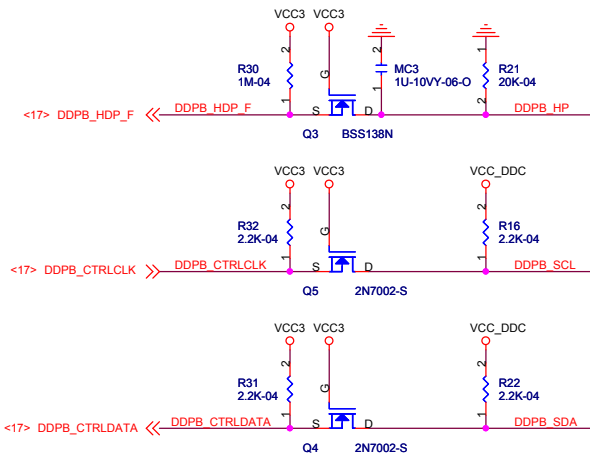
PCI-E X1 B



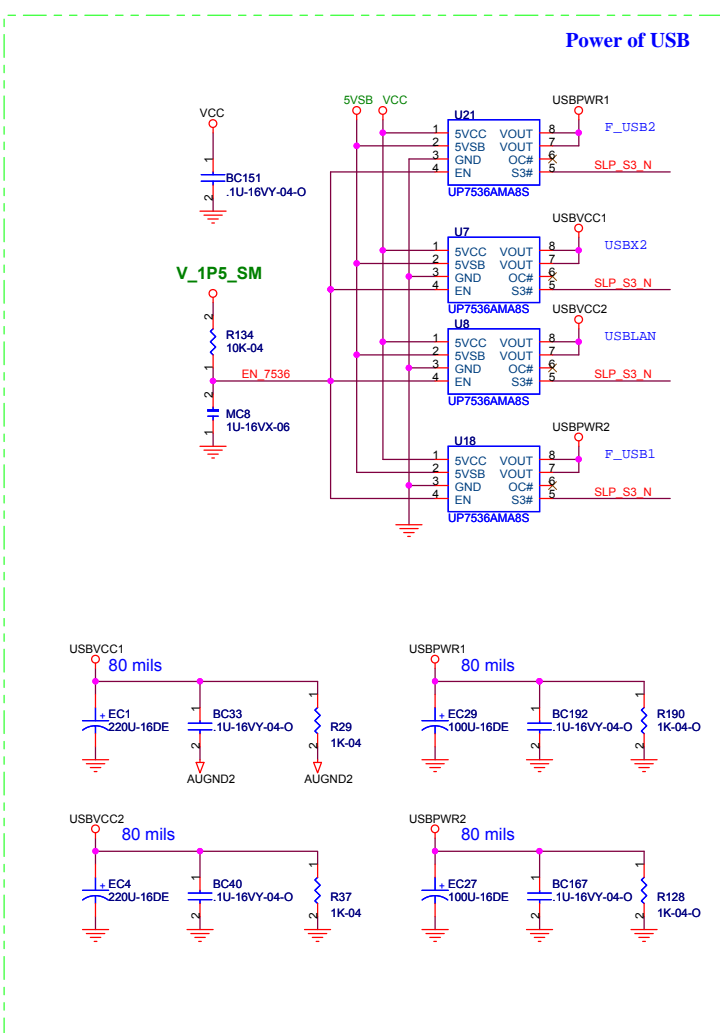
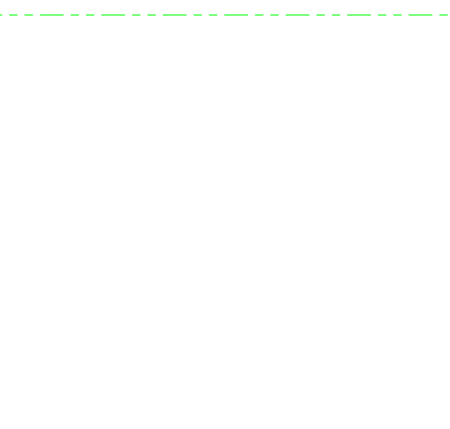
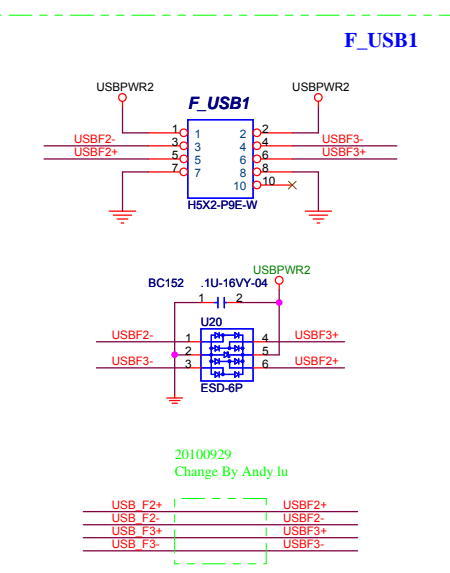
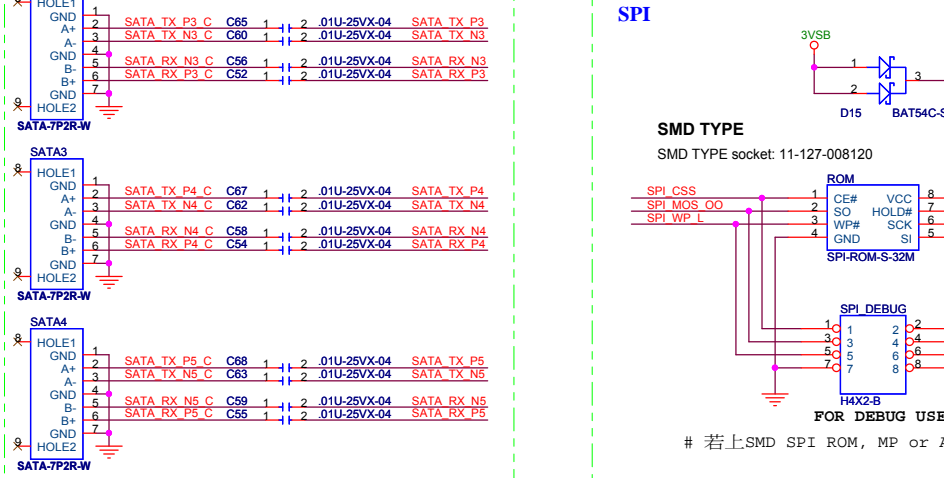
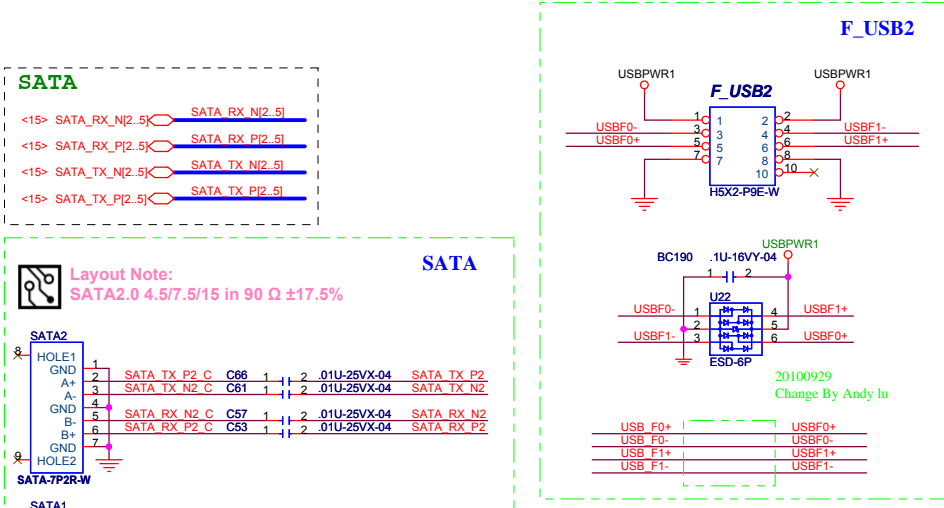
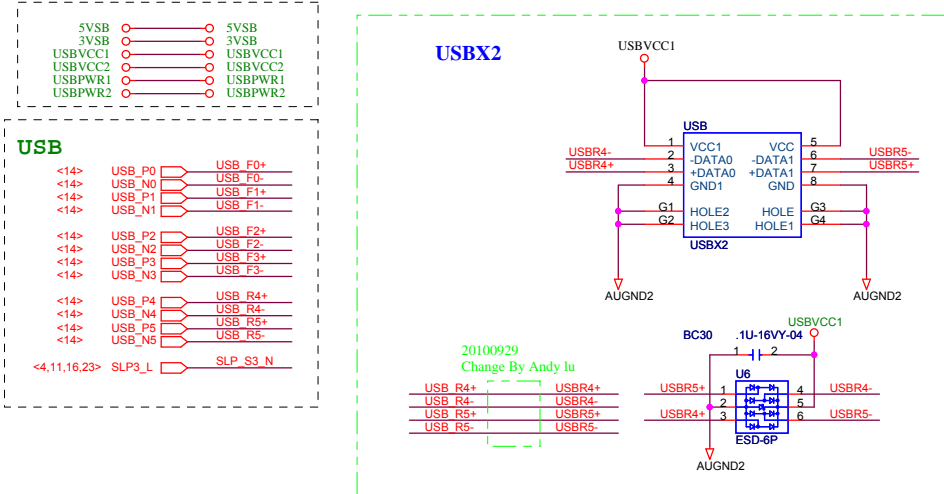
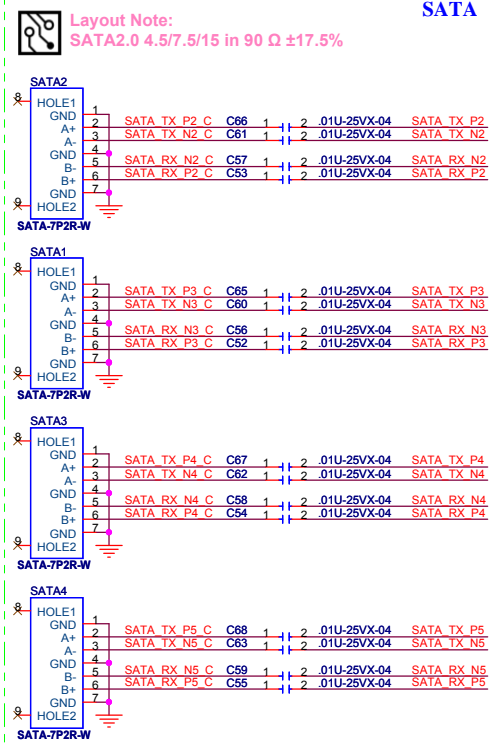
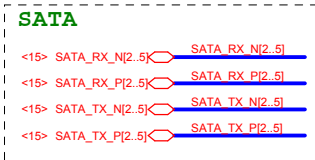
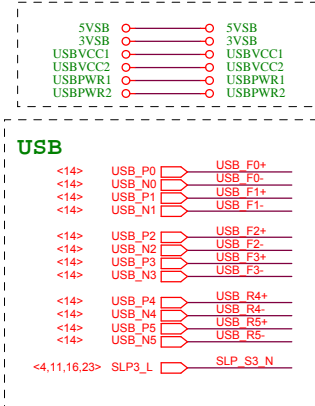
PCI-E X1 A Decoupling Cap.



Between PEX16 & PEX1A

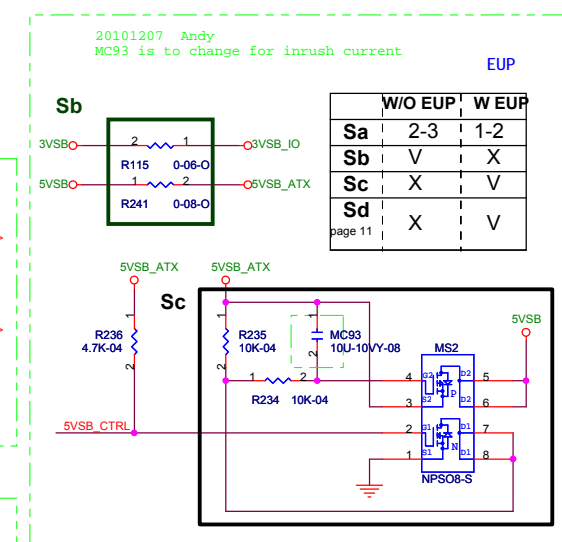
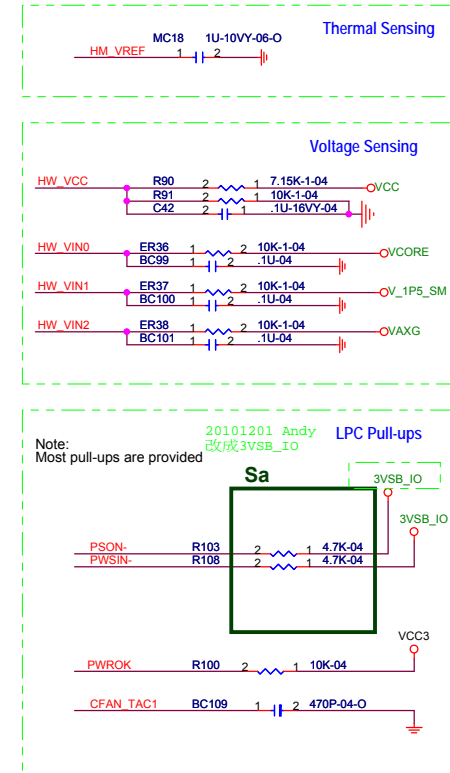
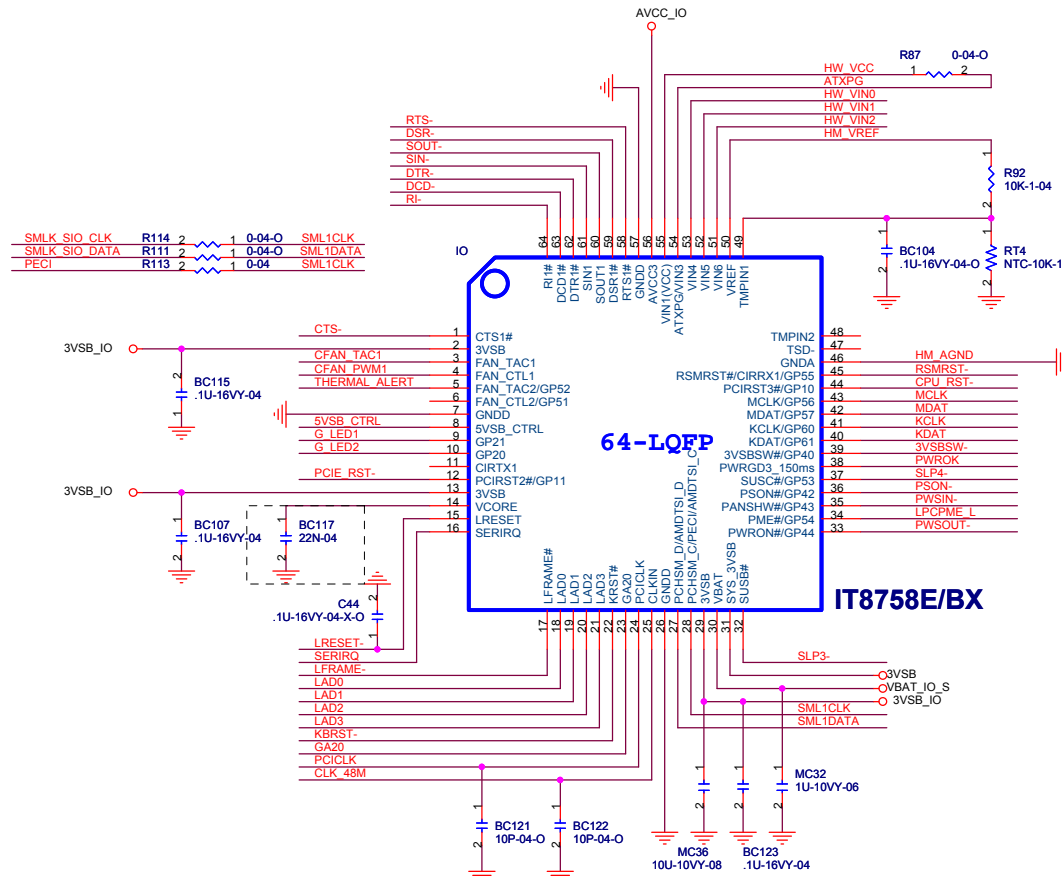
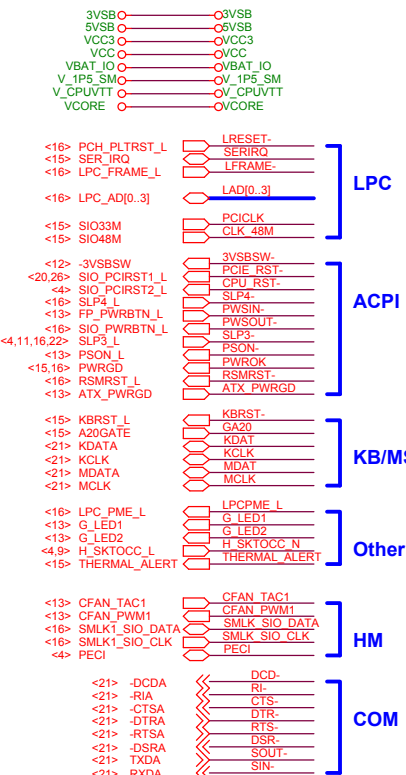






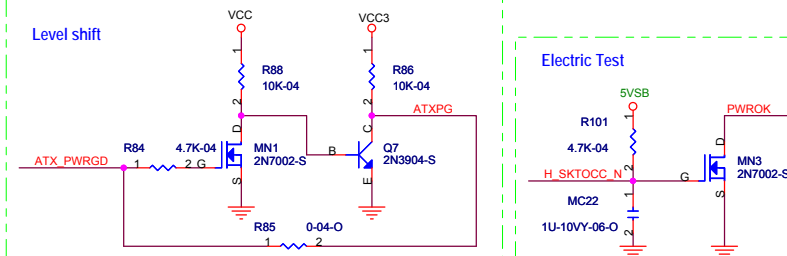


## External Connection

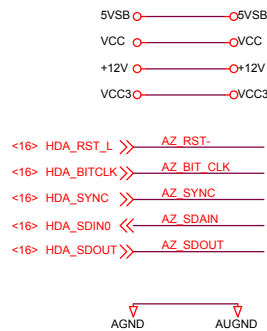


## IT8758 Power On Strapping Options

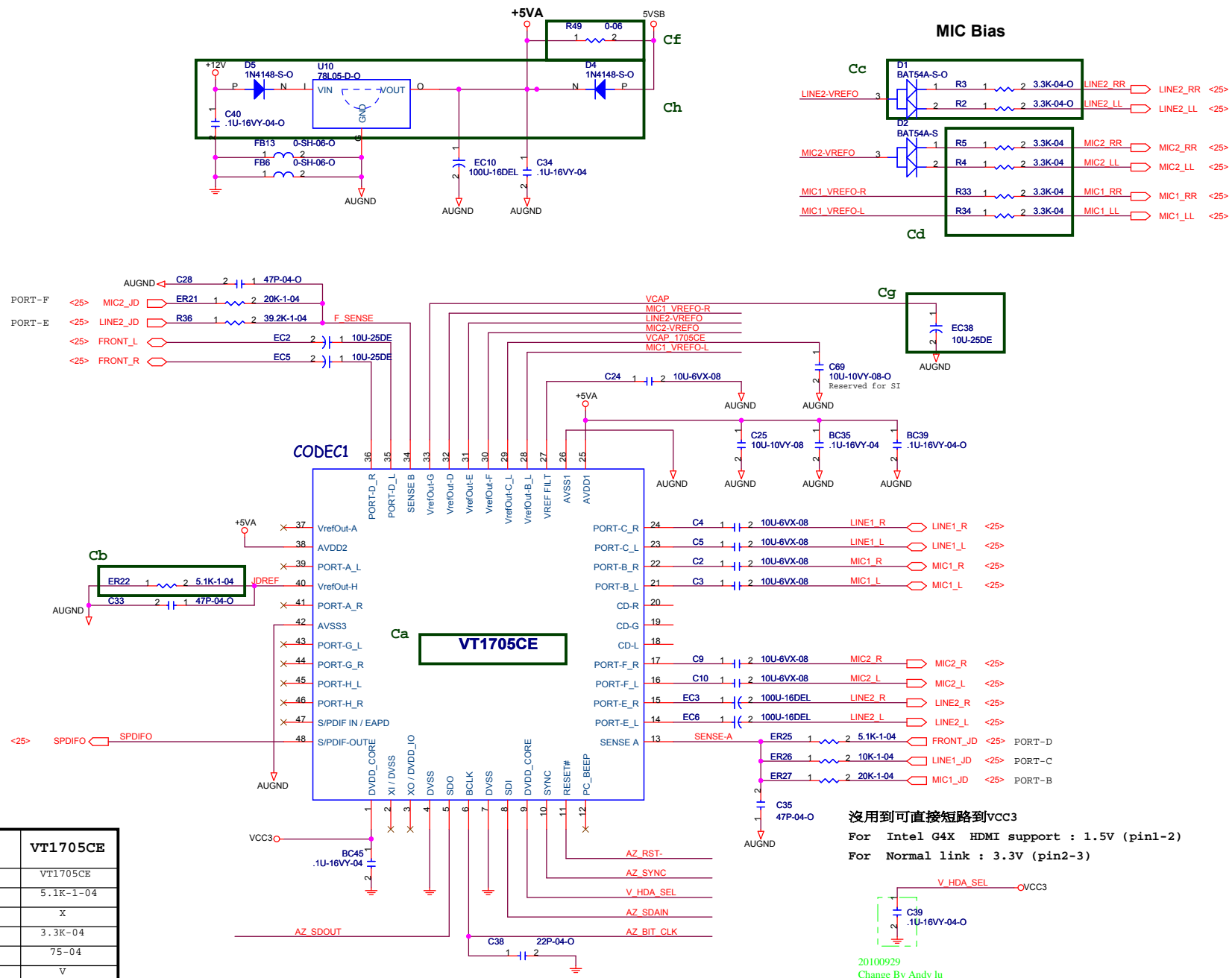
PIN NO.	Symbol	Value	Description
PIN 60	FAN_CTL_SEL	11	The default value of EC Index 63h/6Bh/73h is 80h (50%)
SOUT-		10	The default value of EC Index 63h/6Bh/73h is FFh(Fan off)
PIN 23		01	The default value of EC Index 63h/6Bh/73h is 00h(Fan full speed)
GA20		00	The default value of EC Index 63h/6Bh/73h is 40h



## External Connection



\* VCC1.5 can remove for non-Intel G4X platform



## BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

沒用到可直接短路到VCC3

For Intel G4X HDMI support : 1.5V (pin1-2)

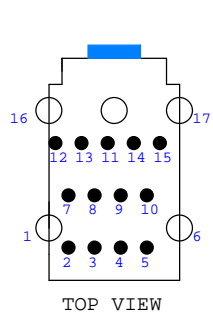
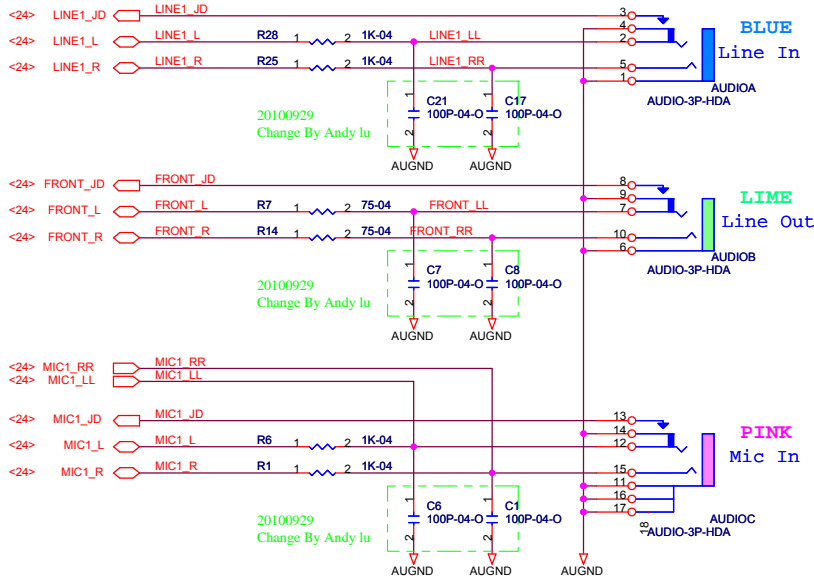
For Normal link : 3.3V (pin2-3)



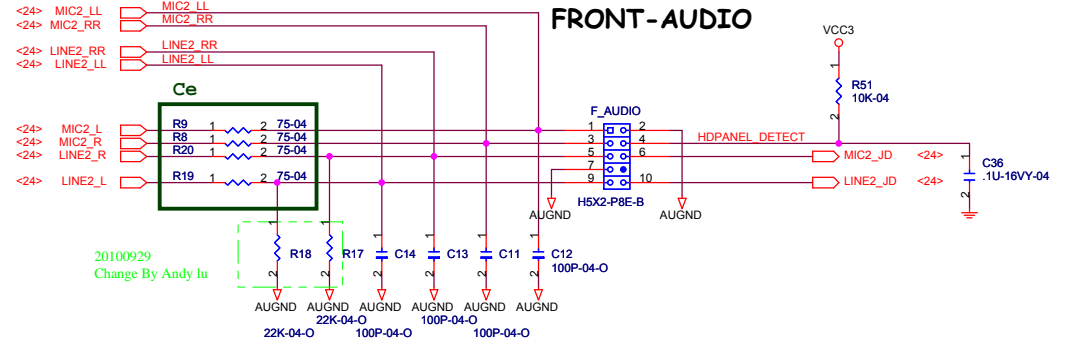
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<16> FP\_AUD\_DETECT << HDPANEL\_DETECT

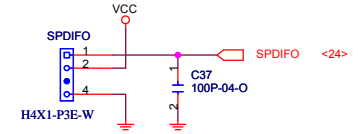
## Non re-tasking for rear panel



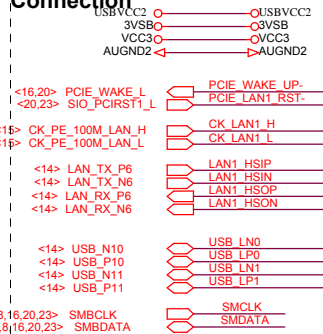
## FRONT-AUDIO



## SPDIF-OUT



## External Connection

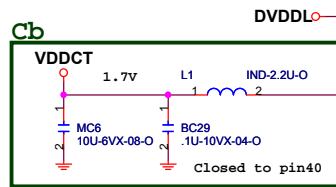


新手提醒： LAN\_HSOP/N請接到SB的PCIE RX端

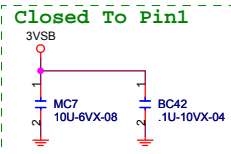
LAN\_HSIP/N請接到SB的PCIE TX端

LAN\_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

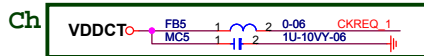
Ch



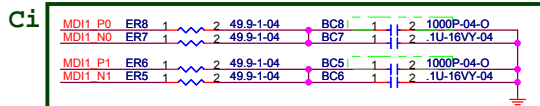
Closed To Pin1



Ch

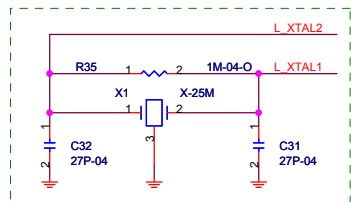
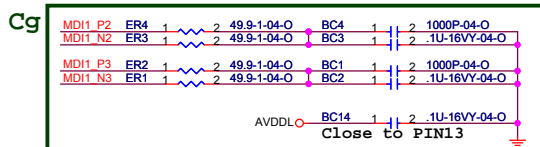


Ch



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Ch

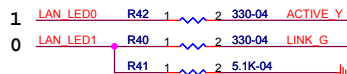


## BOM Difference

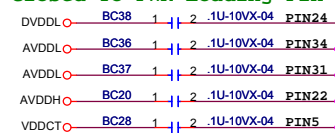
	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Cl	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

## HW Strapping

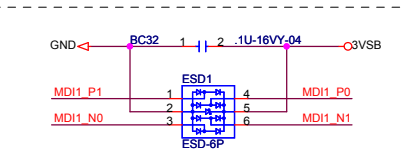
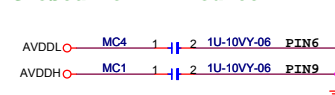
LED0 : 0 -> OC disable  
1 -> OC enable  
LED1 : 0 -> VDDCT\_REG enable  
1 -> VDDCT\_REG disable



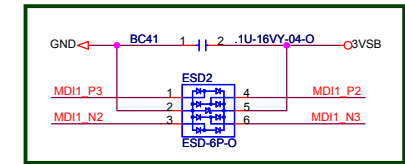
## Closed To PWR Loading Pin



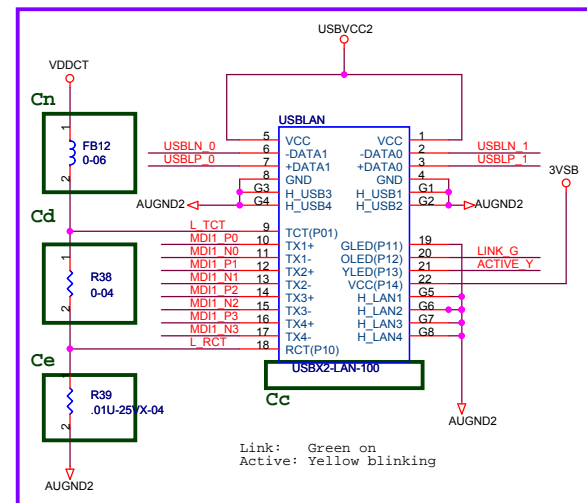
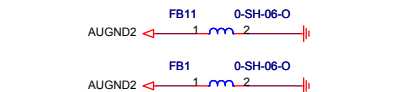
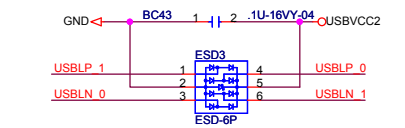
## Closed To PWR Source Pin



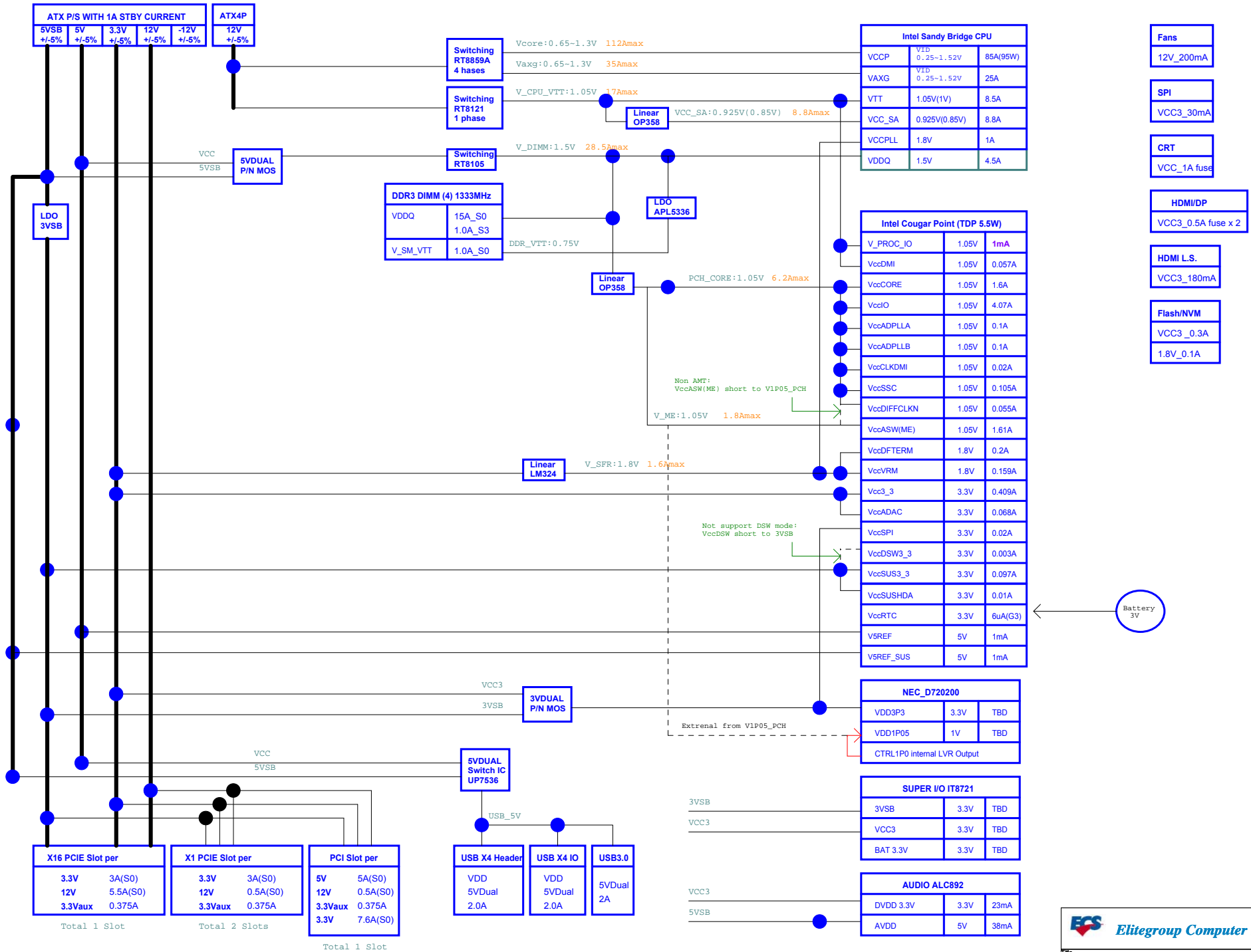
Cf

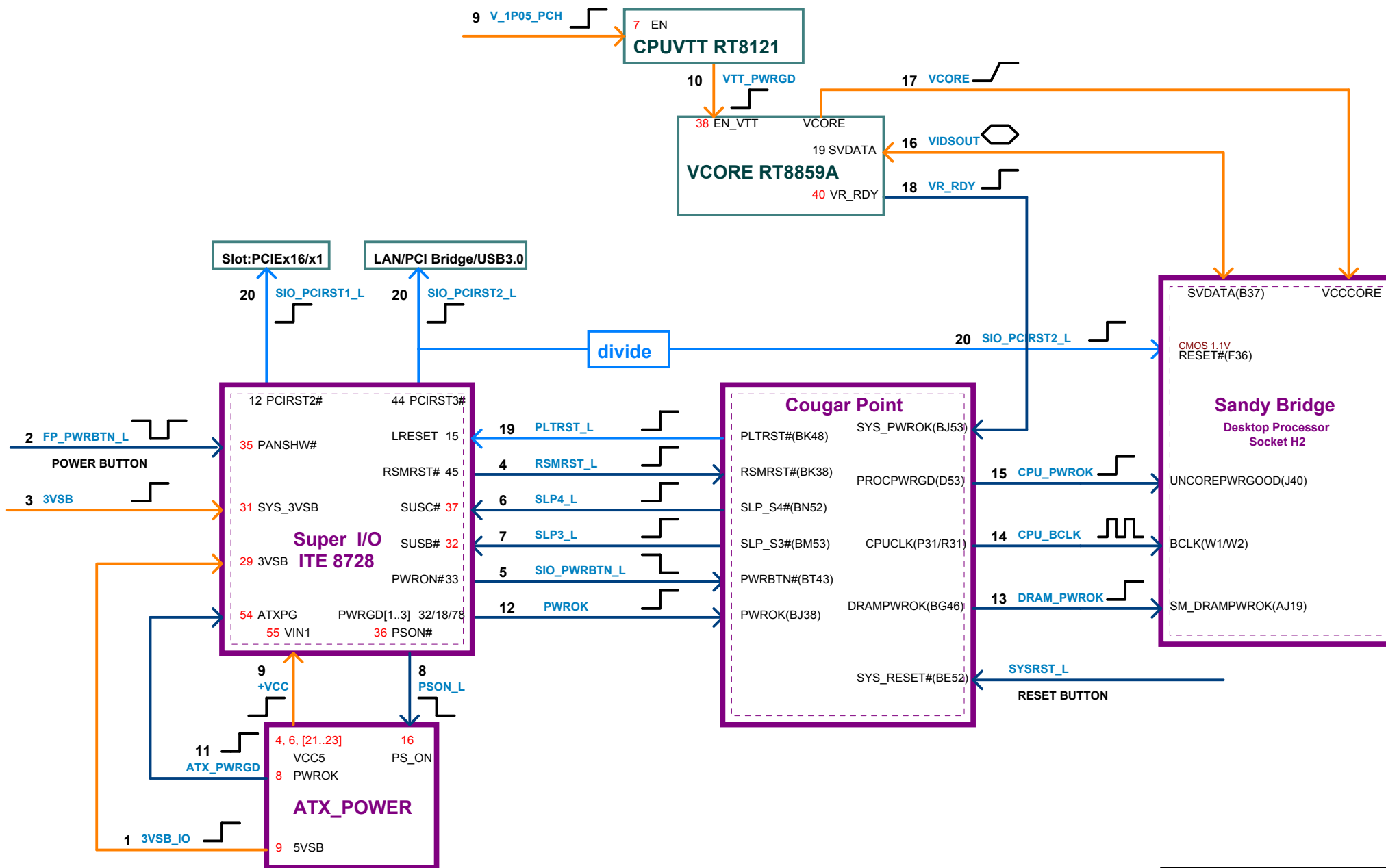


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Link: Green on  
Active: Yellow blinking





**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

